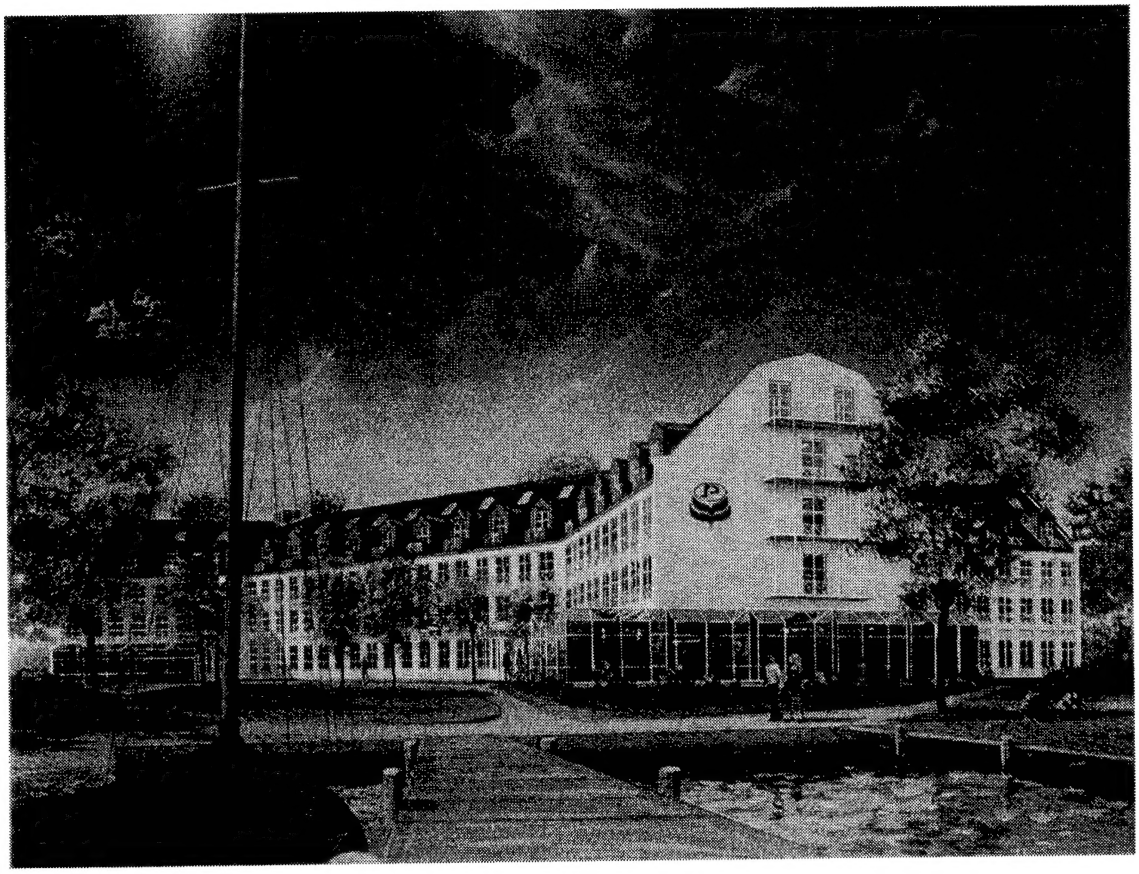

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This is an interdisciplinary conference. Topics include material growth and characterization, recent developments in MESFETS, HEMTs, and HBTs, MMIC-Technology, Microwave and millimeter wave power devices, GaN- Devices, Mesoscopic devices, Optical Ics, Reliability and Characterization, Technological Building Blocks for devices.

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Session 1: Applications

8: 10 **III/V Based MMICs for Microwave links and Multi Media Applications**
H. Dämbkes — *invited*
United Monolithic Semiconductors (UMS), Orsay/ Ulm — France/ Germany

8: 40 **GaAs Monolithic Microwave Integrated Circuits: Application Driven Technology Development**
G. Packeiser — *invited*
Siemens AG, München — Germany

9: 10 **New Satellites for New Services: New Needs for MMICs**
E. Rogeaux, J.-L. Cazaux — *invited*
Alcatel Espace, Toulouse — France

GaAs Monolithic Microwave Integrated Circuits: Application-driven Technology Development

Gerhard Packeiser
Siemens Semiconductor Group

The present situation in GaAs manufacturing is characterized by enormous growth rates in volume production over the past years. The trend is expected to continue. Technology drivers are low-cost implanted MESFET technologies. The most important applications are in the fields of mobile communication systems, hand-sets as well as base stations, satellite communications and radar. Applications are focussed, however, on operation frequencies up to 15 GHz due to the limited f_T-values of standard MESFETs at typically 20 GHz.

As new market segments are evolving, the demand for advanced GaAs technologies is increasing. An application-driven trend towards heterostructure technologies is clearly visible. Mobile communication interlinks, civil as well as military radar systems and smart sensors are driving forces for the expansion of the mass production basis towards HEMT- and HBT-MMICs. Even in future mobile communication systems a couple of novel solutions based on heterostructure MMICs can be anticipated.

The respective systems require a wide range of semiconductor circuit operation frequencies, microwave power levels and/or noise figure performances. For physical reasons not all of these requirements can be covered by one single GaAs technology. So a well-shaped portfolio of technologies in future will be the key to long-term business growth.

The MESFET story is a story of success. It is the most widely used technology for transmitters in L-band mobile communication hand-sets, also in competition with silicon solutions, due to excellent microwave power, efficiency and low cost. A large variety of standard components is available ranging from discrete devices over single-function MMICs towards multifunctional Tx-MMICs. Pre-requisites are a very simple and high yield process (DIOM in case of Siemens), a high volume production line run in the manner of a silicon fab, and low-cost SMD plastic packaging facilities. The very positive development can also be monitored by looking at the production line capabilities: 4" production meanwhile is world standard. The big players including our company are preparing for 6" to take over in less than two years.

The natural expansion into heterostructures starting from MESFET is the HEMT. It is the first active device to cover also millimeterwave applications - on transistor as well as on MMIC level. If optimized well it also provides higher power-added -efficiency in medium or high power devices. For receiver applications, HEMTs offer benefits in noise figure. However, no solution will be achieved without a compromise in device physics. As a consequence the key HEMT applications fall into classes, each of which needs a specifically optimized HEMT technology.

This is why we developed a family of four dedicated - but related - processes, each with a specific and clear application spectrum. They are all based on AlGaAs/InGaAs/GaAs pseudomorphic epitaxial structures. Most processing elements are in common to guarantee for low cost and volume production capabilities. This is why the processes are all based on optical i-line stepper lithography and spacer techniques to define the gate.

HEMT LN60 is the low-noise technology in place for applications up to 40 GHz. It is characterized by a gate length of l_g=180nm yielding f_T=60GHz and f_{max}=120GHz. Typical noise figures NF=0,5dB are achieved at 12GHz and NF=1,3dB at 26GHz, very attractive for receiver applications in general and specifically for satellite communications.

HEMT 110 is the result when tuning pseudomorphic GaAs-basded HEMTs towards highest possible operation frequencies in the range of up to 100 GHz. By applying a gate length l_g=130nm, cut-off frequencies f_T=110GHz and f_{max}≈210GHz are typically being achieved. Depending on the mode of operation and circuit design, devices are perfectly suitable for low noise- (=receive function) as well as power- (=transmit function) applications. This is why HEMT 110 is the technological basis for the ambitious goal to develop a low-cost MMIC-based 77GHz car distance radar for future intelligent cruise control systems. In fact, HEMT technology to date is the only approach to access this frequency band with a monolithic integration concept. The first complete chip-set consisting of amplifiers, mixers and VCO has been demonstrated including receive as well as transmit functions [1]. Even complex multifunction MMICs do not cause principal problems if the transistors are well controlled and precise validated models for the active device as well as the passive structures are available. As an example, the first fully integrated transceiver MMIC has been realized recently [2].

HEMT P60 stands for a power technology with f_T=60 GHz and f_{max}=120GHz. It is designed for high gate-drain breakthrough voltages V_{BD}>9V and operation frequencies up to 40GHz. At a fixed gate length of l_g=180nm the excellent power performance of about 400mW per mm gate width is achieved. Optimization in this case has been carried out on the expense of noise figure. However, comparing power technologies, NF=0,6dB at 12 GHz and NF=1,8dB at 26 GHz is still remarkable. So even transceive MMICs in HEMT P60 technology including power stages are attractive.

HEMT M30 is an approach to satisfy future generation mobile communication demands. Technology requirements are relaxed to end up with f_T=30GHz/f_{max}=60GHz. This is by far enough to cover all L-band systems. The main issues of a mobile com HEMT is its high power added efficiency PAE (60...70%) and - due to its low on-resistance - the capability to operate at supply voltages down to V_{DS}=1,5V. These features are extremely useful for any battery-driven system.

This year, HBT technology based on AlGaAs/GaAs is entering production stage. Mobile communication market will be the first test field. HBT technology has proven to be capable of true 3V operation and high PAE performance [3]. Together with its capability of allowing for very compact power devices and the bipolar-inherent advantage of only one supply voltage needed, it offers high potential for hand-set power applications.

This paper is to illustrate that in industrial III-V-electronics the period of record fishing for example in terms of alternative material systems and device concepts or cut-off frequencies is over. To date the technologies in place cover all important microwave and millimeterwave applications. The real challenge is in performance optimization for the key markets, volume availability and cost.

[1] J. E. Müller, T. Grave, H.J. Siweris, M. Kärner, A. Schäfer, H. Tischer, H. Riechert, L. Schleicher, L. Verweyen, A. Bangert, W. Kellner, Th. Meier: "A GaAs HEMT MMIC chip set for automotive radar systems fabricated by optical stepper lithography", IEEE Journal of Solid State Circuits 32 (1997) 1342

[2] L. Verweyen, H.J. Siweris, M. Neumann, U. Schaper, R. Osorio, A. Werthof, S. Kudszus, H. Massler, H. Tischer, W. Reinert, A. Hülsmann, W.H. Haydl, Th. Meier, W. Kellner, M. Schlechtweg: "Coplanar transceive MMIC for 77GHz automotive applications based on a nonlinear design approach", June 1998 IEEE RFIC Symposium, Baltimore, USA

[3] J.E. Müller, P. Baureis, O. Berger, N. Bovolon, R. Schultheis, G. Packeiser, P. Zwicknagl: "A small chip size 2W, 62% efficient HBT MMIC for 3V PCN applications", to be published in IEEE Journal of Solid State Circuits (1998), special edition on high speed circuits

Session 2: Reliability

10: 10	**Reliability of Compound Semiconductor Power Devices** *W.T. Anderson* Naval Research Laboratory, Washington	*invited* USA
10: 40	**Reliability and Qualification of III/V Semiconductor Devices for Space Applications** *S. Kayali* Jet Propulsion Laboratory, Pasadena, CA	*invited* USA
11: 10	**Electroluminescence Analysis of Multiplication Effects in Pseudomorphic HEMT´s** *G. Meneghesso,* T. Grave, M. Manfredi, M. Pavesi, C. Canali, E. Zanoni Universita di Padova, Padova	 Italy
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11: 30	**Effect of the Surface Recombination on the Base Current of InGaP/GaAs HBTs** R. Plana, *M. Bogarino,* S. Delage, F. Fantini, J. Graffeuil Universita di Parma	 Italy

Reliability of Compound Semiconductor Power Devices

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Although reliability is required by all compound semiconductor devices that are expected to be used in commercial and military systems, by far the most difficult problems are found with the high power devices. This is because, even though the basic designs are the same as for low power devices, such as low noise amplifiers, the high power devices are usually operated at higher current densities, higher internal electric fields, and consequently at higher temperatures.

Reliability work on compound semiconductor devices first concentrated on discrete components such as small signal GaAs field effect transistors (FETs) [1]. A large reliability base now exists for these devices. Less progress has been made on the reliability problems with power GaAs FETs when operated at high bias and input power. Another type of device on which a good deal of reliability work has been directed is the high electron mobility transistor (HEMT) and the later version, the pseudomorphic HEMT or (PHEMT). Heterojunction bipolar transistors (HBTs) have been developed more recently for both microwave power and digital applications; and significant reliability problems have been uncovered, particularly at high power levels.

The first review of compound semiconductor power device reliability (GaAs FETs) was published by Bell Telephone Laboratories [2]. Other recent reviews that emphasize different aspects of reliability are found in references 3-9. The largest programs to study the reliability of GaAs power devices has been the Defence Advanced Research Projects Agency (DARPA) Tri-Service Microwave and Millimeter Wave Integrated Circuits (MIMIC) Reliability and Radiation Effects Program and the Tri-Service Microwave Analog Front End Technology (MAFET) Program. With power Monolithic Microwave Integrated Circuits (MMICs), failure can occur at surfaces and interfaces, in the substrate or active layers, at Schottky barriers, at ohmic contacts, by electromigration, by hot electron effects [8], and by corrosion of the metalizations. As expected, failure usually occurs at the site of the active devices, but this is not always the case.

Important recent problems that are receiving a good deal of attention are hydrogen poisoning of hermetically sealed devices and the lower than expected reliability of HBTs. It has been found that PHEMT based MMICs degrade rapidly due to hydrogen evolution and interaction with the active devices in sealed package, with predicted lifetimes of only 8 years in some applications. Failure mechanisms in HBTs have been studied with respect to material stress[10] and material quality[11] when operated at high current densities. Interdiffusion at interfaces and between metal contacts and the semiconductor may also be a secondary, but still important failure mechanism [12].

References

[1] J.E. Davey and A. Christou, "Reliability and Degradation of Active III-V Semiconductor Devices," in Reliability and Degradation, Semiconductor Devices and Circuits, M.J. Howes and D.V. Morgan, eds. (Wiley, New York, 1981), pp. 237-300.

[2] J.C. Irwin, "The Reliability of GaAs FET's," in GaAs FET Principles and Technology, J.V. DiLorenzo and D.D. Khandelwal, eds. (Artech House, Dedham, MA, 1982), pp. 353-399.

[3] W.T. Anderson, et al., "Subsurface Burnout Mechanisms in GaAs Devices," Quality and Reliability Engineering Intenational, Vol. 4 (1988), pp. 255-268.

[4] S. Adams, et al., "GaAs Reliability and Test," Ch. 6, in Microelectronic Reliability, Vol. I, E.B. Hakim, Ed., (Artech House, Norwood, MA, 1989), pp. 241-311.

[5] D.E. Riva and G.C. Titinet, "Reliability of Compound Semiconductor Microwave Field Effect Devices," Ch. 8, in Microelectronic Reliability, Vol. II, E. Pollino, ed., (Artech House, Norwood, MA, 1989), pp. 195-258.

[6] W.T. Anderson and A. Christou, "Status of Compound Semiconductor Device Reliability,", in Semiconductor Device Reliability, A. Christou and B.A. Unger, eds., (NATO Science Affairs Division and Kluwer Academic Publisher, 1990), pp. 423-437.

[7] F. Fantini and F. Magistrali, "Reliability of Compound Semiconductor Devices, Proceedings of the 2nd European Symposium on the Reliability of Electron Devices, Failure Physics and Analysis (ESREF 1991, Bordeaux, France), pp. 359-376.

[8] E. Zanoni, et al., "Hot-Electron -Induced Effects, Light Emission, Breakdown and Reliability Problems in GaAs MESFET's, AlGaAs HEMT's and AlGaAs/InGaAs Pseudomorphic HEMT's," European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) Proceedings (Glasgow, Scotland, 1994), pp. 261-272.

[9] W. T. Anderson, et al., "Reliability Testing of GaAs MMICs," Proceeding of the 5th International Symposium on the Physical and Failure Analysis of Integrated Circuits, IPFA '95, (IEEE, Singapore, 1995), pp. 161-163.

[10] T. Henderson and T. Kim, "Improved Reliability Self-aligned C/X Monolithic Power HBT Amplifiers Fabricated with A Low Stress Process," Technical Digest, GaAs IC Symposium ,1996, pp. 27-30.

[11] B. Bayraktaroglu, G Dix, S Mohammadi, and D. Pavlidis, "AlGaAs/GaAs HBT Reliability Dependence on Material and Correlation to Baseband Noise," Technical Digest, GaAs IC Symposium ,1997, pp. 157-160.

[12] J.A. Mittereder, J.R. Roussos, and W.T. Anderson, "Reliability Life Testing and Failure Analysis of GaAs Heterojunction Bipolar Transistors," GOMAC '98 Digest of Papers, (Palisades Institute, New York, NY, 1998)

Reliability and Qualification of III/V Semiconductor Devices for Space Applications

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Abstract
This paper provides a description of the reliability and qualification issues related to the application of III/V semiconductor devices in critical space systems. A discussion of common failure mechanisms, radiation effects and other reliability concerns is provided along with a discussion of methods for technology qualification for high reliability space applications.

Introduction
The explosive growth of the WLAN, PCS, DBS, GPS, and cellular telephony markets has resulted in substantial improvements in processing methods, fabrication yield, and overall quality of commercially viable compound semiconductor devices. Many manufacturers now fabricate their standard commercial product line utilizing statistical process control for repeatability and uniformity. This has greatly reduced the infant mortality population without having to impose the traditional high reliability part specification. However, reproducibility of a product does not guarantee reliability in the intended application. For critical space applications where the success or failure of a mission hinges on the lifetime and performance of a single device; It is critical that all aspects of the reliability and the various known failure modes and mechanisms be addressed prior to the insertion of the component in the application [1].

Inasmuch as semiconductor manufacturers have reduced the infant mortality population by improving repeatability in fabricating the devices, the long-term failure mechanisms of compound semiconductor devices cannot be assumed to be predictable based on knowledge of silicon technology. The high reliability user must understand that many of the failure mechanisms associated with silicon devices do not apply to GaAs and other compound semiconductors, and new device structures bring new failure mechanisms. Many of the traditional assumptions for mean-time failure rate predictions do not hold for these new devices. Thus, today's high reliability user must be more aware of measurement based predictions of long term failure rate over calculation based predictions.

Reliability and Failure Mechanisms
Device reliability involves probability statistics, time, and a definition of failure. Given a failure criterion, the most direct way to determine reliability is to submit a large number of samples to actual use conditions and monitor their performance against the failure criteria over time. Since most applications require device lifetimes of many years, this approach is not practical. To acquire device reliability data in a reasonable amount of time, an accelerated life test at high temperatures is used. By exposing the devices to elevated temperatures, it is possible to reduce the time to failure of a component, thereby enabling data to be obtained in a shorter time than would otherwise be required. Such a techniques is known as "accelerated testing" and is widely used throughout the semiconductor industry. The rate at which many chemical processes take place is governed by the Arrhenius equation:

$$R = A \exp(-Ea/kT)$$

Where
R = rate of the process
A = a proportional multiplier
E_a = activation energy, a constant
K = Boltzman's constant, 8.6×10^{-5} (eV/K)

This equation has been adopted by the semiconductor industry as a guideline by which the operation of devices under varying temperature conditions can be monitored. Experimental data obtained from life tests at elevated temperatures are processed via the

Arrhenius equation to obtain a model of device behavior at normal operating temperatures. Rearranging the Arrhenius equation allows the temperature dependence of component failure to be modeled as follows:

$$\ln t_2/t_1 = E_a/k\,(1/T_2 - 1/T_1)$$

where

$t_{1,2}$ = time to failure
E_a = activation energy in electron volts
T = absolute temperature in Kelvin

Failure Modes and Mechanisms:
Failures in electronic devices can be classified as either catastrophic failures or degradation failures. The exact mechanism, which causes the failure is normally dependent on the material structure, processing methods, application, and stress conditions. Device bias, resultant channel temperature, passivation, and material interactions may all cause or contribute to different failure mechanisms. Furthermore, device handling, especially during wire bonding and die attach and packaging may also cause failures [2].

Some of the most common failure mechanisms include:

Gate-Metal Sinking: The performance of GaAs-based devices relies heavily on the quality of the active channel area of the device. The Schottky gate metal-to-semiconductor interface directly influences the device electrical parameters, such as the drain saturation current and reverse breakdown. The gate structures are based on the industry standard multi-layer Au/Pt/Ti or Au/Pd/Ti on GaAs. Inter-diffusion of gate metal with GaAs results in a reduction of the active channel depth and a change in the effective channel doping. This effect is termed "gate sinking." This process is affected by the surface conditions of the GaAs material at the time of deposition, the deposition parameters, and the choice of deposited materials [3,4].

Ohmic Contact Degradation: The most common system for ohmic contacts is AuGe/Ni, which is alloyed into the GaAs at temperatures in excess of 400°C to provide the necessary low contact resistance (0.1 to 0.5 Ω/mm). A thick Au layer is then deposited on top of the alloyed contacts to provide conduction. This structure, employed at the drain and source contacts, has been shown to degrade at elevated temperatures. The degradation is the result of Ga out-diffusion into the top Au layer and the diffusion of Au into the GaAs causing an increase in the contact resistance. The Ni layer used in the ohmic contact is intended as a Au- and Ga-diffusion barrier. Some other materials such as Cr, Ag, Pt, Ta, and Ti have been used as barrier materials with varying degrees of success. The activation energy associated with ohmic contact degradation varies between 0.5 eV and 1.8 eV. This activation energy may provide reasonable contact life at low operating temperatures (<100 °C) but it also indicates rapid deterioration at elevated temperatures [5].

Channel Degradation: Degradation observed in device parameters can sometimes be attributed to changes in the quality and purity of the active channel area and a reduction in the carrier concentration beneath the gate Schottky contact area. These changes have been postulated to be a result of diffusion of dopants out of the channel or diffusion of impurities or defects from the substrate to the channel. Deep level traps have also been postulated to cause similar degradation in MESFETs.

HEMT devices, being strongly dependent on the properties of the interface of the AlGaAs/GaAs heterostructure, can suffer a related failure mechanism. A decrease in electron concentration in the channel, caused by a de-confinement of the 2DEG, was postulated to be the cause of the observed failure mechanism.

HEMT devices can also suffer from metal-diffusion-related mechanisms, which are manifested as channel-related degradation. Lateral diffusion of Al into the gate recess region changes the conduction band discontinuity and consequently the confinement of the channel electrons. Gold diffusion from the ohmic contact into the active channel region under the gate can also cause similar degradation. Lastly, vertical diffusion of Al from the AlGaAs donor layer and Si from the n^+ AlGaAs layer into the channel layer causes an increase in the impurity scattering in the undoped GaAs, thus deteriorating the high electron mobility of the 2DEG [6].

Surface State Effects: The performance of GaAs-based devices depends highly on the quality of the interface between metal and GaAs or the

passivation layer (Si_3N_4 or SiO_2) and GaAs. The quality of the interface can depend on the surface cleaning materials and procedures, the deposition method and conditions, and the composition of the passivation layer. The main effect of an increase in surface state density is the lowering of the effective electric field at the drain/gate region, which results in an increase in the depletion region and a change in the breakdown voltage.

Unpassivated devices can be susceptible to surface oxidation and loss of arsenic, which may result in an increase in gate leakage current and a reduction of the breakdown voltage. Devices passivated using SiO_2 may experience surface erosion due to the interaction of SiO_2 with GaAs [7].

Electromigration: The movement of metal atoms along a metallic strip due to momentum exchange with electrons is termed electromigration. Since the mechanism is dependent on momentum transfer from electrons, electromigration is dependent on the temperature and number of electrons. Therefore, this failure mechanism is generally seen in narrow gates and in power devices where the current density is greater than $2x10^5$ A/cm^2, which is normally used as a threshold current density for electromigration to occur. This effect is observed both perpendicular and along the source and drain contact edges and also at the interconnect of multilevel metallizations.

The metal atoms that migrate along the line tend to accumulate at the grain boundaries. The accumulation of metal at the end of the gate or drain contact can create fingers of metal that can short the device. Material accumulation and void formation perpendicular to the source and drain contacts can cause hillock formation over the gate structure. This may result in shorting the gate to the source or drain which may result in catastrophic failure.

Hot Electron Trapping: Under RF drive, hot electrons are generated near the drain end of the channel where the electrical field is the highest. A few electrons can accumulate sufficient energy to tunnel into the Si_3N_4 passivation to form permanent traps. These traps can result in lower open-channel drain current and transconductance, and higher knee voltage, leakage current, and breakdown voltage. Since the traps are located above the channel, there is usually little change in the dc or small signal parameters near the quiescent point. Further, since the traps are located beside the channel, Schottky-barrier height and the ideality factor often remain constant. This selective change in device characteristics helps distinguish hot-electron effects from thermal or environmental effects [8].

Hydrogen Effects: Degradation in I_{DSS}, V_p, g_m, and output power was observed on GaAs and InP devices tested in hermetically sealed packages or under hydrogen atmosphere. The source of the degradation has been attributed to hydrogen gas desorbed from the package metals (Kovar, plating, etc.). The exact mechanism by which hydrogen degrades the device performance and the path by which hydrogen reaches the active area of a device are not known and have been under investigation [9].

Earlier research on GaAs transistors identified the diffusion of atomic hydrogen directly into the channel area of the device where it neutralizes the silicon donors as the possible mechanism. It is believed that atomic hydrogen diffuses into the GaAs channel and forms Si-H, thereby neutralizing the donors. Experiments have shown that exposure of Si-doped GaAs to RF hydrogen plasma results in neutralization of the Si donors. Infrared spectroscopy data have also given evidence of $(SiAs_3)As$-H complexes.

The neutralization of donors can decrease the carrier concentration in the channel, which, in turn, can decrease the drain current, transconductance, and gain of the device. Hydrogen effects in FETs with either Pt or Pd gate metals have been observed. Recent research has concluded that the diffusion of hydrogen may occur at the Pt side-walls and not at the Au surface of the Au/Pt/Ti gate metal.

Other research on GaAs PHEMT and InP HEMT in a hydrogen atmosphere has shown that the drain current may increase in some cases. This observation has led to the conclusion that the hydrogen diffuses into the semiconductor surface where it is thought to change the metal-semiconductor built-in potential.

Manufacturers and users of GaAs devices used in hermetically sealed packages are currently pursuing an acceptable solution to this problem. Some of the possible solutions include thermal treatment of the packaging materials to reduce

the amount of desorbed hydrogen after the seal, the use of hydrogen getter materials in hermetically sealed packages, and the use of barrier materials that do not contain the Pt/Ti or Pd/Ti structure. These solutions have limitations and possible instability problems that must be fully understood prior to implementation in high reliability systems.

Qualification:
Qualification can be defined as the verification that a particular component's design, fabrication, workmanship, and application are suitable and adequate to assure the operation and survivability under the required environmental and performance conditions.

Traditional qualification methods require extensive test and characterization of the specific component using a predetermined set of tests and characterization conditions. This approach has been very costly in schedule and expense and typically results in very little interaction between the device manufacturer and the user.

A methodology for qualification based on continual interaction between the device manufacturer and the user is described in this paper. This interaction results in a detailed understanding of the device design, fabrication, and limitations along with the specific application conditions and expected operating environment. The methodology is divided into three main categories; Process Qualification, Product Qualification, and Product Acceptance.

Process Qualification: Is a set of procedures the manufacturer follows to demonstrate the control of the entire process of design and fabrication using a specific technology (MESFET, HEMT, HBT, etc.). It addresses all aspects of the process including the acceptance of starting materials, documentation of procedures, implementation of handling procedures and the establishment of lifetime and failure data for devices fabricated using the process. Since the goal of process qualification is to provide assurance that a particular process is under control and known to produce reliable parts, it needs to be performed only once, although routine monitoring of the production line is standard. It is critical to remember that only the process and basic circuit components are being qualified. No reliability information is obtained for particular component designs.

Although process qualification is intended to qualify a defined fabrication procedure and device family, it must be understood that the technology is constantly evolving, and this technology evolution requires the continual change of fabrication procedures. Thus, strict application of the commonly used phrase, "freezing the production process," does not apply.

The qualification process also involves a series of tests designed to characterize the technology being qualified. This includes the electrical as well as the reliability characteristics of components fabricated on the line. Some of these tests are performed at wafer level and include the characterization of Process Monitors (PM), and Technology Characterization Vehicles (TCV). Others tests require the mounting of circuits or elements into carriers. All of these tests and the applicable procedures are an integral part of the qualification program and provide valuable reliability and performance data at various stages in the manufacturing process.

Product Qualification: is the verification that a component will satisfy the design and application requirements under the specified conditions. The information sought after in this approach is design specific and applies to devices fabricated on qualified process lines. This qualification step is composed of Design Verification and Product Characterization.

Design Verification is one of the best ways of reducing engineering costs and improving reliability. Design reviews with the participation of the device manufacturer and the device user is one of the means of accomplishing this verification of model or simulation and layout of the design prior to fabrication.

Product characterization is another important aspect of product qualification. Thermal analysis and test to determine the thermal characteristics of the design, along with ESD sensitivity tests, voltage ramp tests, and temperature ramp tests are all essential in obtaining an understanding of the limitations and characteristics of the design.

Product Acceptance: Although devices may be designed by highly qualified personnel, fabricated on a process qualified production line, and verified through measurements to meet the design goals, parts with poor reliability characteristics still may exist. This may be due to

Electroluminescence analysis of multiplication effects in pseudomorphic HEMT's

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Mastering hot-electron and impact-ionization effects is of crucial importance for the design of power AlGaAs/InGaAs pseudomorphic HEMT's. The pile-up of generated holes in the gate-source region and/or the injection of holes in the buffer or donor layers have been claimed to cause I_D and output conductance increase observed when impact-ionization takes place, but this has never demonstrated experimentally [1]. This pseudo-bipolar effect leads to a positive feedback mechanisms, which could possibly explain the recent observations of on-state breakdown burnout occurring when a certain level of impact-ionization current is reached [2, 3].

Spectroscopic analysis of electroluminescence (EL) has been extensively used to characterize hot carrier effects in MESFET's and HEMT's [4, 5]. In this paper we analyze carrier transport phenomena occurring in pseudomorphic AlGaAs/InGaAs HEMT's biased in the on-state impact-ionization regime by means of EL. In particular: (i) we confirm the presence, in the electroluminescence spectra of pseudomorphic HEMT's, of a dominant contribution at high energies due to electron-hole recombination, and we identify a composite peak due to the recombination of cold carriers; (ii) we analyze the recombination peak using a high-resolution monochromator, which reveals the fine structure due to transitions between electron and hole subbands in the channel quantum well, thus providing useful data concerning the properties of the InGaAs HEMT channel. The EL data are modeled by means of a self consistent tight binding calculation [6]; (iii) we observe that the fine structure of the recombination peaks is not influenced by the drain-source voltage, thus suggesting that recombination occurs between non-energetic electrons and holes in the gate-source region, as observed by N. Shigekawa et al. [7] for InAlAs/InGaAs HEMT's on InP; (iv) we also show, for the first time, that at high V_{DS} and electric field, significant recombination occurs in the AlGaAs layers, which demonstrates the real space transfer of both electrons and holes.

Devices used in this work where 0.25 μm double heterojunction AlGaAs/InGaAs/AlGaAs pseudomorphic HEMT's (PM-HEMT's). The bell-shaped behaviour of I_G as a function of V_{GS} is the typical signature of impact-ionization, see Fig.1 [1]. For V_{GS} > -0.1 V the decrease in the gate-drain electric field, together with the possible transfer of electrons to the AlGaAs layer both contribute to lower the impact-ionization rate down to very low values. At decreasing the temperature, the gate current and the multiplication ratio $|I_G|/I_D$ (not shown) increase due to the reduced phonon scattering and to the improved electron transport properties, which lead to more energetic electrons. We analyzed the EL radiation emitted by the devices under test, biased at high V_{DS}, in the 1.1 - 2.6 eV range. Figure 2 shows the electroluminescence spectra taken at 160 K in a device biased at V_{GS} = -0.3 V from V_{DS} = 6 V to V_{DS} = 9 V. The most interesting feature of the spectra are two recombination peaks at $\simeq$ 1.3 eV and $\simeq$ 1.7 eV. The shape of the 1.3 eV recombination peak does not change at increasing the drain-source voltage. Only the intensity increases, following the increase in the hole current generated by impact-ionization. Beyond V_{DS} = 7 V a peak at E $\simeq$ 1.7 eV appears, which corresponds to band-to-band recombination in the AlGaAs. The peak at 1.3 eV was analyzed at a higher energy resolution (0.003 eV), see Fig.3 and Fig.4. Three different peaks have been identified, corresponding to radiative recombination between conduction and valence subbands in the InGaAs quantum well [6, 8]. The energy of the peaks shifts towards higher values as the temperature is decreased, following the corresponding increase in the $In_{0.2}Ga_{0.8}As$ energy gap variation, see Fig.5 [9], with a temperature coefficient of about 0.4 meV/K. Figure 6 shows the experimental data taken at V_{DS} = 9.3 V, together with the calculated EL spectra as obtained by self-consistent tight binding calculation [6]. Figure 3 demonstrate that the shape of the recombination peak does not change with V_{DS}, despite the fact that the relative intensity of the various contributions is extremely dependent on the band bending. Figure 7 shows that the EL intensity and the hole current-drain current product ($I_G \cdot I_D$) are proportional, thus demonstrating that recombination is the dominant mechanism for light emission. Figure 8 shows EL spectra for different V_{GS} at V_{DS}=9.3 V, T=160 K. The behavior of the intensity of the emitted radiation is not monotonic and drops below of the sensitivity of the detection system for V_{GS} > 0.2 V, despite the maximum I_D is measured in these conditions.

In conclusion, the data presented here demonstrate that EL spectra of PM-HEMT's biased at high V_{DS} are dominated by electron-hole recombination. By analyzing at high resolution peaks due to recombination in the channel and donor layers, useful information concerning hole transport, which determines device breakdown and burnout, can be obtained. In particular it is shown that most of the recombination occurs in the gate-source region, where hole pile-up may occur. Furthermore, evidence of holes and electrons real space transfer in the donor layer is provided by the observation of a $\simeq$ 1.7 eV recombination peak, corresponding to the AlGaAs energy gap. Differently from photoluminescence, the described technique can be applied to completed devices in operating conditions.

This work was partially supported by the European Research Office of the US-ARMY under the contract N68171-97-C-9034

[1] A. Neviani et al., J. of Appl. Phys. (6), p. 4213, 1993. [2] H. Rohdin et al., proc of IPRM, p. 357, 1997. [3] M. H. Somerville et al., proc. of IEDM, p. 553, 1997. [4] C. Tedesco et al. IEEE-Trans. on El. Dev. (40), 1211, 1993. [5] H. P. Zappe et al., Appl. Phys. Lett., (59), p. 2257, 1991. [6] A. Di Carlo et al., Sol. State Com., (98) p. 803, 1996. [7] N. Shigekawa et al., IEEE El. Dev. Lett. (16), p. 515, 1995. [8] F. Aniel et al., J. of Appl. Phys., (77), p. 2184, 1995. [9] Properties of lattice matched and strained Indium Gallium Arsenide, edited by B. Bhattacharya, published by INSPEC, the institute of El. Engin. London, U.K.

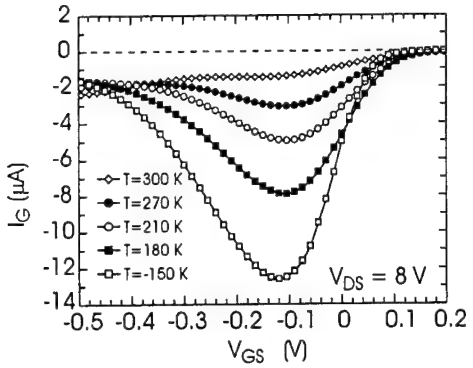

Fig.1 I_G vs. V_{GS} as a function of temperature in a typical device.

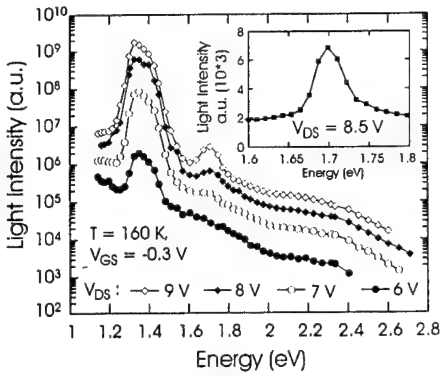

Fig.2 Electroluminescence spectra for different V_{DS} measured at 160 K.

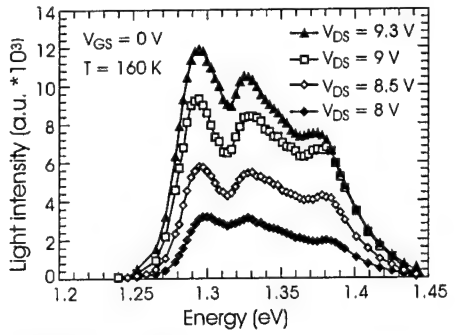

Fig.3 High resolution analyses of the channel recombination peak, measured at different V_{DS} values.

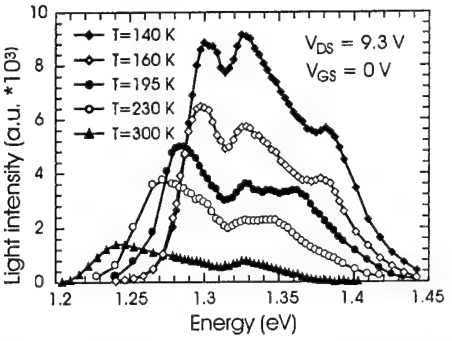

Fig.4 High resolution analyses of the channel recombination peak measured at different measured at different ambient temperatures.

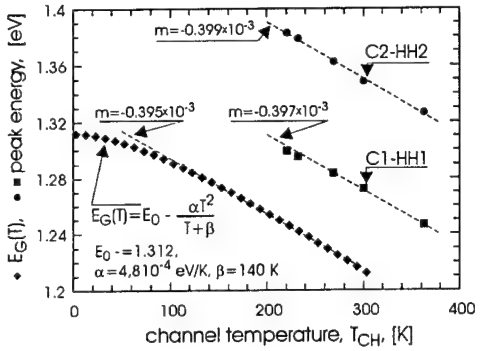

Fig.5 Recombination peaks energy and $In_{0.2}Ga_{0.8}As$ energy gap variation as a function of channel temperature, as reported in [9].

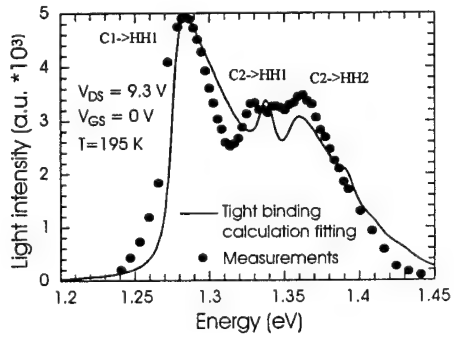

Fig.6 Comparison between electroluminescence data and results of tight binding calculation at V_{DS}=9.3 V, T=195 K.

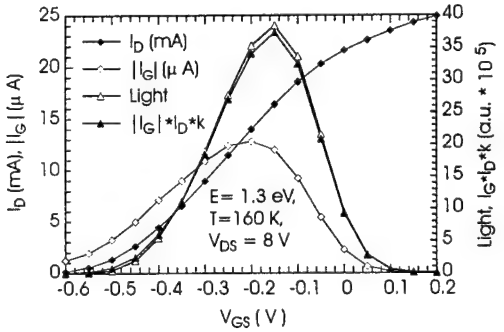

Fig.7 I_D, $|I_G|$, $|I_G| \cdot I_D$ and light intensity at 1.3 eV as a function of V_{GS} measured at V_{DS}=8 V, T = 160 K.

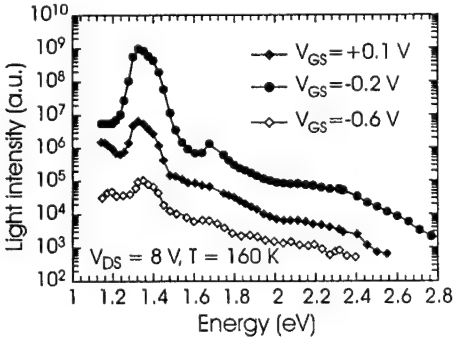

Fig.8 Electroluminescence spectra at various V_{GS} at V_{DS}=9.3 V, T=160 K.

Millimeter Wave InP HEMT MMIC Technology: Thermal Stability and Performance

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InP-based HEMTs have to date demonstrated the best high frequency characteristics of any transistor, including the highest f_t and f_{max}, the lowest noise figure and the highest efficiencies for power amplification. These characteristics make them the best technology choice for several advanced systems for space and military applications, such as smart munitions, passive imaging and radiometry, and commercial applications such as automotive radar. Unfortunately, the relative immaturity of InP-based HEMT processing technology, in comparison to GaAs PHEMTs, limits its introduction into systems. Consequently, much effort is being directed towards the development of reliability and manufacturability of the InP-based HEMT MMICs. Here, we will demonstrate the fabrication and the design of W-band high gain passivated 0.15 µm double side doped InAlAs/InGaAs HEMTs, with a high uniformity and yield over 2'' InP substrates. By using this technology, a single stage amplifier with 10.2 dB gain at 88 GHz and a distributed amplifier with 11 dB gain and 89 GHz bandwidth were demonstrated. Furthermore, the robustness of our InP-based HEMTs MMICs technology will be demonstrated by high temperature stress.

The epitaxial structures used in this work were grown on 2 inch InP substrates. The schematic cross section of the epitaxial structure is illustrated in fig. 1. The process flow of our W-band MMICs and device fabrication is shown in fig. 2. Typical output I-V characteristics of our passivated 0.15 µm InP-based HEMTs are shown in fig. 3. The wafer average peak-g_m at 1 V drain bias exhibits 800 mS/mm, with a standard deviation of 30 mS/mm. The average threshold voltage across the wafer is -900 mV, with a standard deviation of 50 mV. The average f_T at V_{ds}=1 V is 158 GHz, with an f_{max} of 310 GHz and standard deviations of 10 GHz. These devices show very low gate leakage current of 4-6 µA/mm, and drain-gate breakdown voltage of about 5 Volts. These characteristics demonstrate the excellent uniformity of our MBE growth, the high selectivity of our gate-recess etching process and the high quality of our PECVD silicon nitride.

The f_{max} of the InP-based HEMTs is mainly limited by the gate-drain feed-back capacitance. This feed-back capacitance depends on the gate recess design, the thickness of the silicon nitride passivation layer and the shape of the gate (T or Y). Figure 4 shows the extracted C_{gd} versus gate widths for 0.15µm InAlAs/InGaAs HEMTs, with and without passivation. The C_{gd} extracted at V_{ds}=2 V from active InP-based HEMTs devices is identical with the C_{gd} extracted from the devices made on semi-insulating GaAs substrates. This proves that at V_{ds}=2 V, C_{gd} is mainly related to the capacitance due to the gate-drain metallization. Without passivation, the intrinsic gate-drain feed-back capacitance is about 30 fF/mm, and 45 fF/mm with passivation. Thus, our SiN passivation introduces a low parasitic capacitance of 15 fF/mm. Extremely high gains of 11.5 dB measured at 94 GHz and 10 dB at 120 GHz were achieved with 0.15 µm passivated devices at V_{ds}=1.5 V, giving an f_{max} exceeding 380 GHz.

To demonstrate the high gain of our 0.15 µm InP-based HEMT technology at W-band, a single stage amplifier was fabricated using only series transmission lines for input and output matching. A small signal gain of 10.2 dB was achieved at 88 GHz for 0.15 µm passivated InP HEMTs, as shown in fig.5-a. This high gain shows the capabilities of our passivated 0.15 µm InP-based HEMTs to provide useful gain at W-band and beyond. We have also fabricated a four-stage distributed amplifier with 11 dB gain and 89 GHz bandwidth, as shown in fig. 5-b.

Figure 5 shows the robustness of our InP-based HEMTs technology in a test at 230°C for 130 hours in nitrogen ambient. Although the passivated devices did not show any change in DC characteristics, such as the peak g_m and the source and drain resistances, as shown in fig. 6. This proves the excellent thermal stability of the ohmic contact and interface silicon-nitride/GaInAs cap-layer. The gate leakage current measured at V_{ds}=1 V at peak g_m increases only slightly and no significant shift in threshold voltage is found. These results show that, the PECVD silicon nitride deposition is a very promising technique for passivation of InAlAs/InGaAs HEMTs.

WOCSDICE'98, Berlin, 24-27 May 1998.

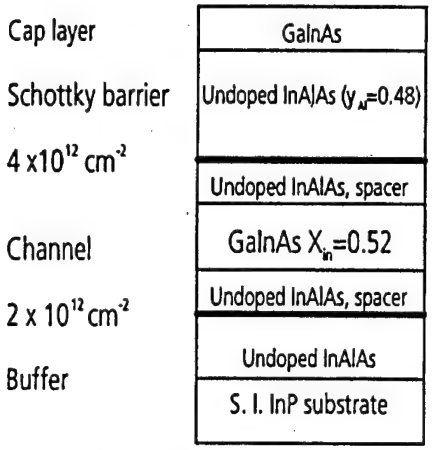

Fig.1: Cross sectional of HEMT layers for a device lattice matched to InP substrate.

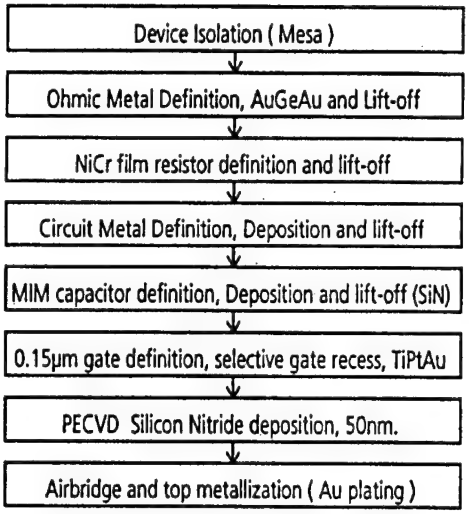

Fig.2: Process flow of W-band MMIC process.

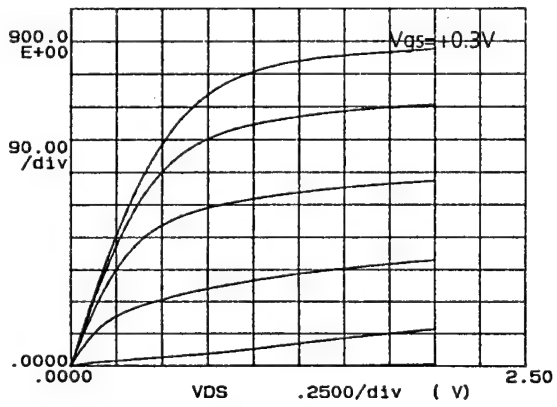

Fig: 3: I-V characteristics of passivated 0.15 µm passivated InP-based-HEMT, with gate bias steps of -0.3 V.

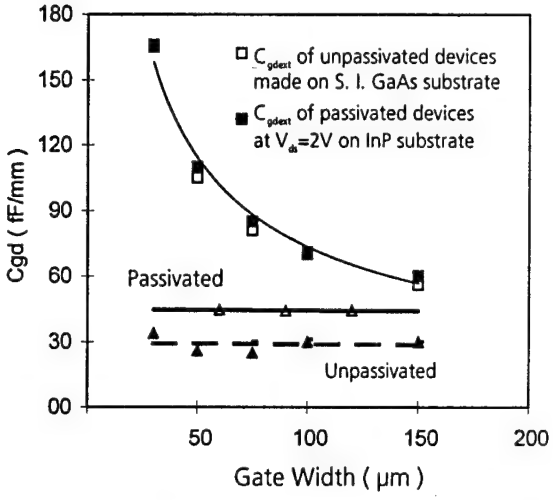

Fig. 4: Comparison of the extracted C_{gd} on 0.15 µm HEMTs on InP and semi-insulating GaAs substrates. The effect of silicone nitride on the intrinsic C_{gd} is shown.

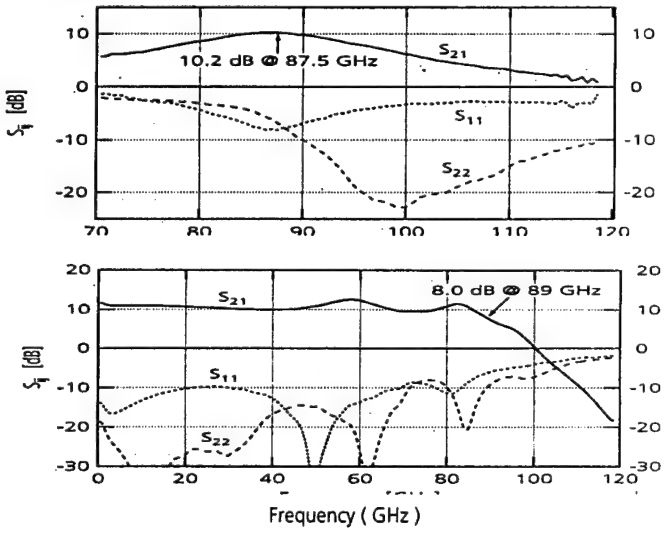

Fig. 5: Measured small signal gains and return losses of single stage amplifier (top), and four stage distributed amplifier (bottom).

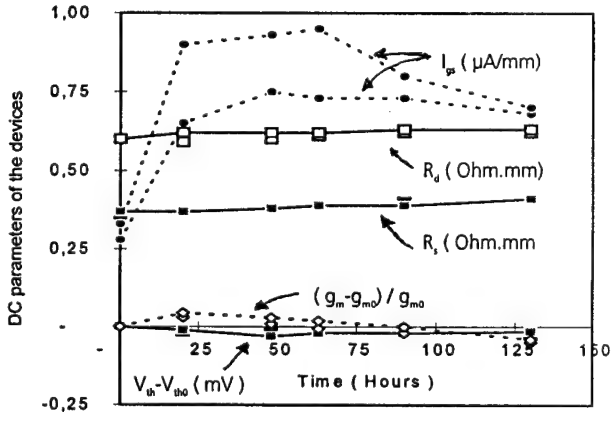

Fig. 6: DC parameters of 0.15 µm InP-based HEMTs after storage test in nitrogen ambient at 230 °C.

EFFECT OF THE SURFACE RECOMBINATION ON THE BASE CURRENT OF GaInP/GaAs HBTs.

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During the early phase of a stress test with the devices biased in the Forward Active Region, we observed a current gain increase in C-doped GaInP/GaAs HBTs. This behaviour is known in the literature as the burn-in effect. Two different technological solutions for the surface passivation were applied: the first one is the standard SiN passivation (sample A) and the second alternative is the edge-ledged technique (sample C). The structure of the samples is depicted in Fig. 1. All the devices were MOCVD grown, double mesa processed and not-self aligned. The standard devices were available in three different emitter width ($W_E = 1\mu m, 2\mu m, 3\mu m$) while for the edge-ledged W_E was only $2\mu m$. For all the devices, both cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) were larger than 40GHz.
The forward Gummel plots indicated that the A samples exhibited a base current higher than C samples; the ideality factor of the base current was 1.30 and 1.60 for the A and C samples, respectively. Since the extrinsic base surface recombination gives rise to an ideality factor ranging between 1 and 1.33 and the space charge region recombination gives rise to an ideality factor of about 2 [1], the lower value of η_B in the A samples indicates that the surface recombination current components were higher. This agrees with the large emitter-size effect [2] exhibited by the A samples (Fig. 2). After the pre-stress characterization, we stressed the devices by biasing the transistors in the forward active region. During the test, we fixed the collector emitter voltage $V_{CE} = 7.70V$ and the collector current density $J_C = 1.7 \cdot 10^4 A/cm^2$. As a consequence of the stress, we observed a decrease of the base current, which was much larger for A HBTs than for C HBTs. In addition, we stressed the A samples by leaving the collector terminal floating and biasing in the forward mode the base-emitter junction; the stress current density was kept to $J_C = 2.0 \cdot 10^4 A/cm^2$. In this case, we observed a reduction of the emitter-size effect (see Fig. 3). The base current variations were attributed to a reduction of the extrinsic base surface recombination current [3], because the emitter-size effect decreased with the stress time. In point of fact, we observed also a decrease of the lorentzian component of the input noise voltage generator. In conclusion by our results, we demonstrated that the edge-ledge passivated devices are much less affected by the surface recombination and, therefore, by the burn-in effect.

[1] W.Liu, E.Beam, T.Henderson, S.K.Fan, "Extrinsic Base Surface Passivation in GaInP/GaAs Heterojunction Bipolar Transistor" *IEEE Electron Device Lett.*, vol. 14, no. 6, 1993, pp. 301-303.

[2] T.S.Hiraoka, J.Yoshida, M.Azuma, "Two Dimensional Analysis of Emitter-Size Effect on Current Gain for GaAlAs/GaAs HBTs", *IEEE Trans. on Electron Device*, Vol. ED-34, No. 4, April 1987, pp. 721-725 .

[3] N.Hayama, K.Honjo, "Emitter Size Effect on Current Gain in Fully Self-Aligned AlGaAs/GaAs HBTs with AlGaAs/GaAs Surface Passivation Layer", *IEEE Electron Device Lett.*, Vol. 11, No. 9, September 1990, pp. 388-390

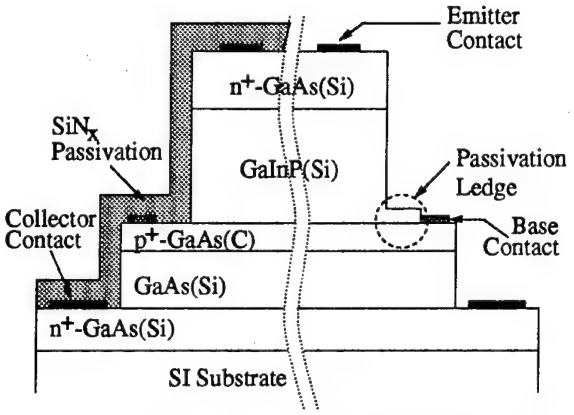

Figure 1: Epitaxial structure of the investigated HBTs.

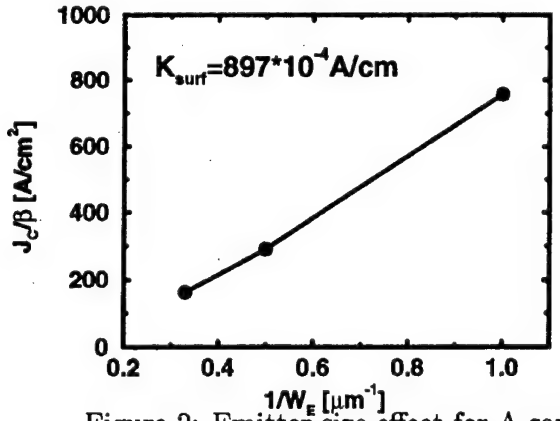

Figure 2: Emitter-size effect for A samples.

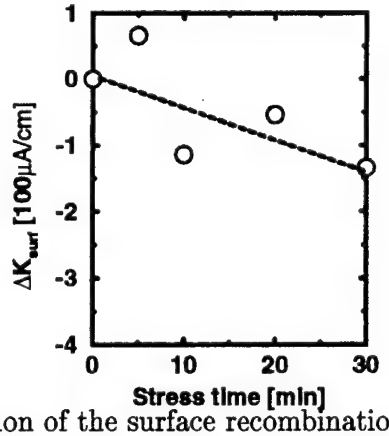

Figure 3: Reduction of the surface recombination current for A samples.

Session 3: Technology and Material Characterization

11: 40	**100 mm Substrates in Metalorganic Vapor Phase Epitaxy Production Systems** *R. Beccard,* H. Protzmann, D. Schmitz, G. Strauch, M. Deschler, M. Heuken, H. Jürgensen AIXTRON AG, Aachen	Germany
11: 50	**GaInP/GaAs HBT Technology Using TBA, TBP, Precursors and Application to Optoelectronic Circuits** J.W. Park, S. Mohammadi, *D. Pavlidis* University of Michigan, Ann Arbor, Mi	USA
12: 00	**SEM-EBIC Study of Defect Distribution in GaAs Structures Irradiated by Low-Energy Ions** *G.N. Panin,* O.V. Kononenko, V.V. Valyaev, V.T. Volkov, V.N. Matveev Institute of Microelectronics Technology and High Purity Materials, Chernogolovka	Russia
12: 10	**Photoluminescence Characterisation of Semi-Insulating GaAs Materials** *F.V. Motsnyi,* V.I. Bosyi, O.I. Eremenko, A.V. Ivazchuk, V.G. Komarov, V.F. Motsnyi, L.G. Shepel, O.S. Zinets National Academy of Sciences of Ukraine, Kiev	Ukrainia
12: 20	**Characterization of Residual Carbon in Undoped Semi-Insulating GaAs by Low Temperature (77K) Photoluminescence** *K.D. Glinchuk,* N.M. Litovchenko, A.V. Prokhorovich, O.N. Striluk National Academy of Sciences of Ukraine, Kiev	Ukrainia
12: 30	**AFM and STM Characterisation of Porous Gallium Phosphide** *V.M. Ichizli,* M. Kuhne, I.M. Tiginyanu, H.L. Hartnagel TU Darmstadt	Germany
12: 40	**Plasma Enhanced Chemical Vapour Deposition of Tungsten Silicide Thin Film on GaAs** S. McClatchie, *D.V. Morgan,* H. Thomas University of Wales, Cardiff	UK

22nd Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe
(WOCSDICE '98)
Zeuthen, Germany, May 24-27, 1998

GaInP/GaAs HBT Technology Using TBA, TBP Precursors and Application to Optoelectronic Circuits

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GaInP/GaAs technology is nowadays generally accepted as a good alternative to AlGaAs/GaAs due to the absence of Al and the good etching selectivity of GaInP over GaAs. Since the first demonstration of GaInP HBTs by MOCVD by UofM/Thomson, important progress was made in hydride-free grown materials and devices. This paper reports the development of Chemical-Beam-Epitaxy (CBE) based technology using TBA, TBP, tDMAAs precursors and its application to HBTs and optoelectronic circuits.

The GaInP HBTs had a 7000Å n-GaAs collector (1.5 x $10^{16}cm^{-3}$) followed by a 600Å p^+ GaAs base (4 x $10^{19}cm^{-3}$) and a tunneling emitter. TBA and TBP were precracked while tDMAAs was injected at room temperature. H_2S and TMGa were used for n and p-doping respectively. The use of tDMAAs allows drastic reduction of sulfur incorporation compared with TBA and thus a very low residual carbon doping ($<10^{15}cm^{-3}$) could be achieved in the collector. Total defect density lower than $10def/cm^2$ was possible with the developed process. Minimum drift of growth parameters was also demonstrated i.e., ~0.27% change of growth rate per month.

The fabricated devices had non-alloyed Ti/Pt/Au for emitter and Pt/Ti/Pt/Au was used for the base. Laterally etched undercut was used for in the base-collector region to reduce the base-collector capacitance while avoiding resistance degradation. HBTs with $2\times30\mu m^2$ emitters had current gain cutoff frequency (f_T) of 60GHz and maximum oscillation frequency (f_{max}) of 100GHz. First reliability tests performed on these devices showed minimum degradation of DC characteristics upon DC bias stress.

Transimpedance amplifiers were designed based on the small- and large-signal characteristics of discrete GaInP HBTs. The basic design had a common-emitter gain stage and the fabricated chips showed a transimpedance gain of 45dBΩ with a bandwidth of 10GHz. A cascode design was also explored for the gain stage and resulted in 47dBΩ gain with 19GHz bandwidth. This design was also found to be less sensitive to large-signal operation due to smaller self-biasing. Eye pattern tests confirmed operation of the transimpedance amplifiers up to at least 10Gbit/sec.

Overall, we present the development of hydride–free CBE technology with highly reproducible growth characteristics and suitability for HBT layer growth. Use of this technology led to good high frequency device performance and reliable characteristics under DC bias stress. Optoelectronic circuits built with such HBTs allowed demonstration of Gbit operation.

Work supported by CNET France-Telecom/DRI, Thomson-CSF, ARO-URI and DARPA-COST

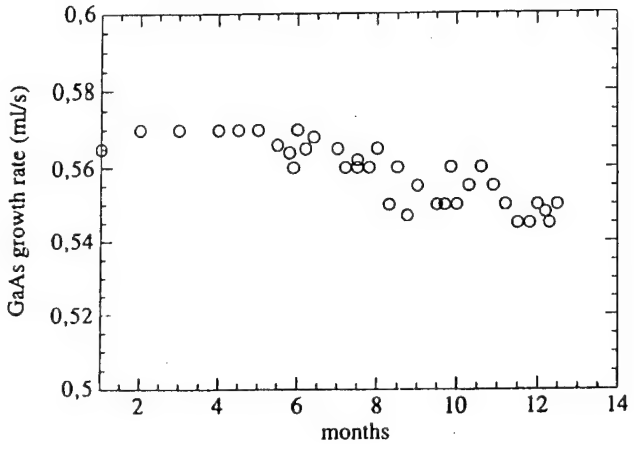

Fig. 1 Growth reproducibility demonstrated by the evolution of growth rate during a period of 12 months at a fixed temperature and TEG pressure set pointA

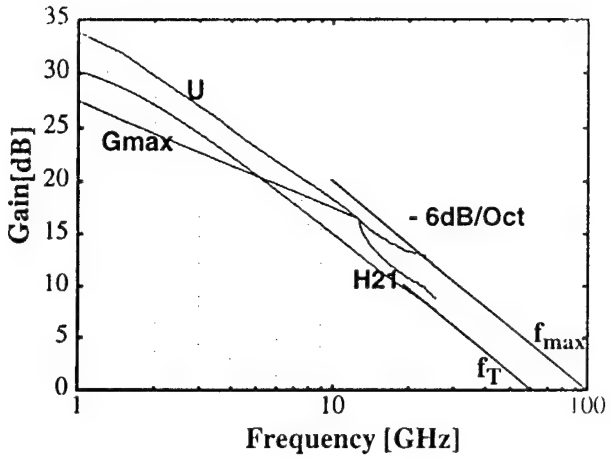

Fig. 2: High-frequency performance of 2×30μm HBT at V_{CE}=3V and I_C=20mA

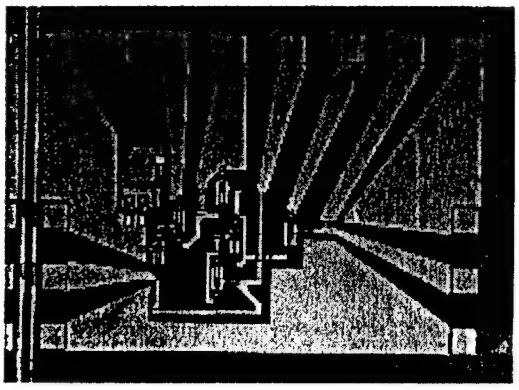

Fig. 3 Photograph of the fabricated transimpedance amplifier with cascode gain stage

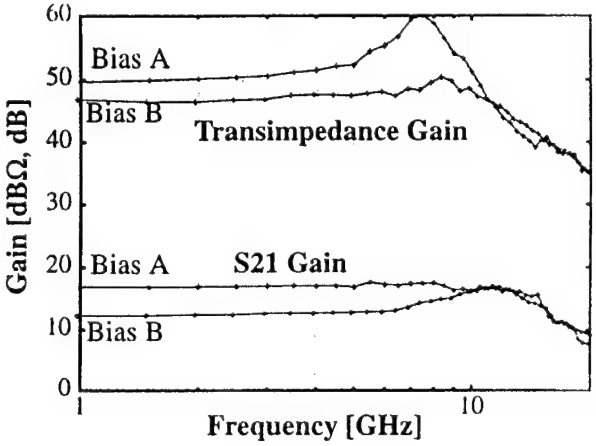

Fig. 4 Transimpedance and S_{21} gain of the cascode amplifier under different bias conditions

SEM-EBIC STUDY OF DEFECT DISTRIBUTION IN GaAs STRUCTURES IRRADIATED BY LOW-ENERGY IONS.

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Low-energy ion bombardments such as reactive ion etching, ion beam milling, ion assisted deposition etc. have been widely used to fabricate semiconductor fine structures and devices. At the ion energy used in these advanced applications, most of the ion energy is deposited within 5-10 nm of the surface. However, a much more extended defect profile is revealed in optical and electrical measurements of processed semiconductors. Distributions of defects are reported to have exponential tails extending tens of times deeper than the mean ion range.

In the present paper, an electron beam induced current (EBIC) technique in a scanning electron microscope was used to reveal a spatial distribution of electrically active defects induced by the Au ions bombardment of MOCVD GaAs films during the Au contact deposition. Subsurface layers of the films were δ-doped with Si up to 8.0×10^{12} cm^{-2} to create n^+-layer. The n^+/n^--GaAs films of 180 nm thickness were grown on the GaAs substrate with a buffer layer of 500 nm thickness. Au depositions onto the film surface were made by an electron beam deposition technique and by a partially ionised beam (PIB) with accelerating voltage up to 6 kV at vacuum of 10^{-8} Torr.

EBIC images show a more homogeneous defect distribution in Au/GaAs structures prepared by PIB compared with the electron beam deposition method. At the last case, recombination active extended defects were revealed. However, the Au ion bombardment has been found to introduce electrically active point defects extending unexpectedly far from a bombardment region. EBIC profiles acquired at different parameters of an incident electron beam by scanning of Au/GaAs contacts indicate that during irradiation both shallow and deep centres are created within a region significantly extending the ion penetration range. It has been shown that a lateral induced defect distribution can extend up to hundreds micrometers reducing nonmonotonically an efficiency of charge carriers collection.

PHOTOLUMINESCENCE CHARACTERISATION OF SEMI-INSULATING GaAs MATERIALS

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Semi-insulating gallium arsenide are widely used in modern semiconductor device technology for fabrication of ultra high frequency devices (FET with the Schottky barrier, avalanche-transit and Gunn diodes, VLCI, bistabile devices etc.), which require high structural and topological perfection of crystals. To satisfy these requirements the detail study of interaction of impurities and intrinsic defects which are introduced in the crystal lattice at various technological operations (the crystal growth, the ion implantation, annealing, the surface treatment) is needed.

In the present work we have studied the low temperature photoluminescence spectra of semi-insulating GaAs crystals of different types (laboratory production: AR-19, AR-40; and commercial: AGP-2, AGP-3, AGP-4, AGP-5, AGCP-3, AGCP-4, AGCP-5, AGCP-5V), grown by Czochralski method at different technological conditions. The obtained data allow to conclude that carbon is one of the main background impurities in such materials. The structure perfection significantly aggravates under the traditional high temperature annealing of semi-insulating GaAs wafers because near the surface the creation of conductive layers with thickness of several microns takes place.

We have registered the fine structure of the edge band 1.514 eV and the impurity band 1.490 eV. This structure caused by a) polariton emission from upper and low polariton branches; b) radiative recombination of free holes on shallow neutral donors (D^o,h); c) radiative recombination of excitons bound to shallow neutral donors (D^o,X) and to shallow carbon acceptors (C^o_{AS},X); d) excitons bound to the point structure defects (d,X); e) electron transitions between the conduction band and shallow neutral carbon acceptor; f) the electron transitions between

donor-acceptor pairs in which carbon and possibly zinc are acceptors in the ground $1S_{3/2}$ state.

We have investigated the lux-intensity dependencies of the lines caused by polariton emission from the upper polariton branch and photoluminescence of (D^o,h), (C^o_{AS},X), (d,X) complexes. The experimental characteristics are satisfactory agree with the theoretical one. We have shown that one of the best available semi-insulating GaAs materials is a new commercial AGCP-5V material which differs from others by considerable concentration of shallow donors and new acceptors beside with the known shallow C^o_{AS} acceptor centres.

We have studied also the influence of the quality of semi-insulating GaAs substrates on the gain and the noise figure of FET. For transistors made from the best material the gain is higher by 1.2-0.8 dB than in other materials and the noise level is lower by 0.3-0.5 dB at the frequencies 8-18 GHz. For the frequency 36 GHz the influence of quality of materials on the transistor parameters is even more significant.

CHARACTERIZATION OF RESIDUAL CARBON IN UNDOPED SEMI - INSULATING GaAs BY LOW TEMPERATURE (77K) PHOTOLUMINESCENCE

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Undoped semi-insulating (s.-i.) GaAs substrates (the resistivity $\rho = 1 \cdot 10^8$ Ohm·cm at 300 K and $\rho = \infty$ at 77 K) are widely used for fabrication of high-speed metal-semiconductor field-effect transistor integrated circuits(MESFET IC). Threshold voltages of MESFET IC depend on the residual carbon content in the substrates, so it is important to know the carbon concentration N in the GaAs substrate. Carbon - induced localized vibrational mode (LVM) absorption measurements are commonly used to find the carbon concentration in undoped GaAs. Some deficiencies associated with the use of this technique exist. So it would be helpful to have available an alternative method to determine the carbon content. Just such alternative photoluminescence (PL) method is presented in our report. The reach the aim the 77K PL spectra of undoped s.-i. GaAs crystals with the known amount of carbon atoms was studied and analyzed. The main attention was paid to the peak intensities of the carbon-induced emission band I_{ca}*(peaked at $h\nu_m = 1.489$ eV) and the near-intrinsic emission band I_i* (peaked at $h\nu_m = 1.508$ eV). As a result the calibration curves I_{ca}^* / I_i^* vs. N for the determination of the carbon content in undoped s.-i. GaAs crystals were obtained (see Fig.1). The calibration curves could be approximated by the following relation:

$$N_c = (8.1 \pm 2.8) \cdot 10^{16} \frac{I_c^*}{I_i^*} \text{cm}^{-3}$$

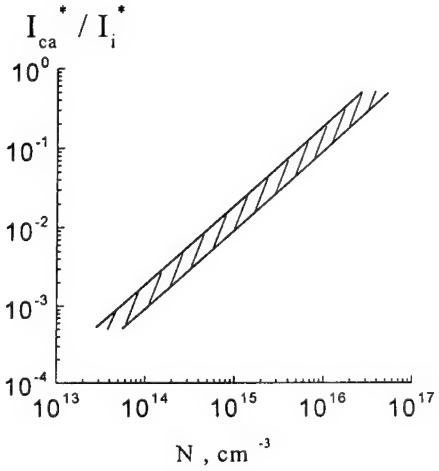

Fig.1. Calibration dependences I_{ca}^*/ I_i^* vs. N for carbon atoms in undoped s.-i. GaAs crystals

The carbon content obtained by the proposed method agree well with that obtained by the LVM absorption method. But in contrast to the LVM absorption technique the PL technique do not need thick samples and no complex measurement instrumentation.

AFM and STM characterisation of porous gallium phosphide

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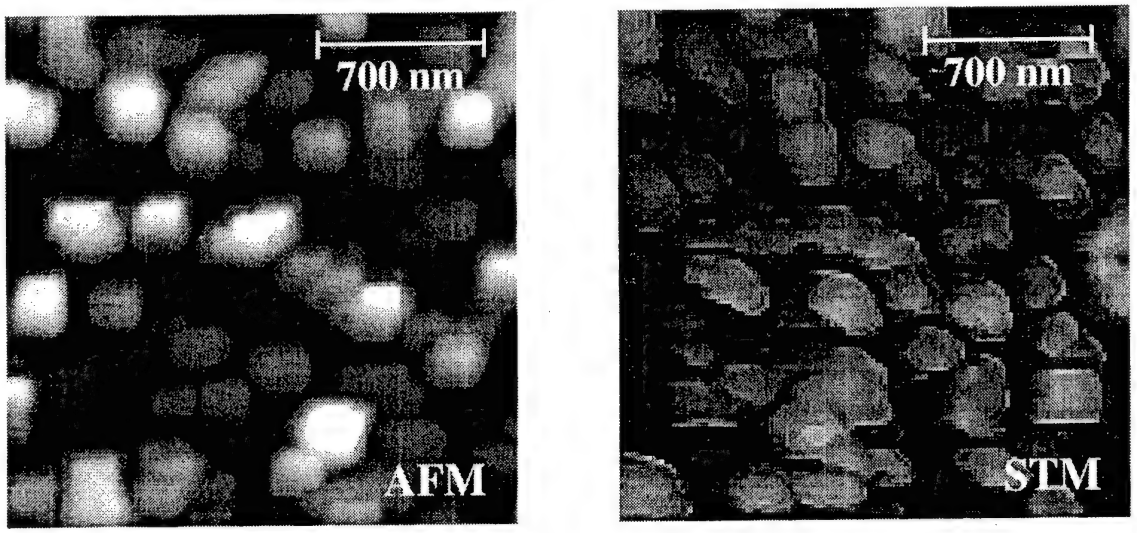
Since porous Si was discovered by Canham [1] to emit visible light, porous semiconductors have attracted a great interest. Besides elementary semiconductors, porous compound semiconductors are being involved in recent investigations. III-V compounds, especially gallium phosphide, in their porous state were found to have unique properties that significantly differ from those of porous Si. One of these properties is surface morphology [2-4].

Among well known techniques that are used to image porous morphology are Scanning Tunneling Microscopy (STM), Atomic Force Microscopy (AFM), and Scanning Electron Microscopy (SEM). The present work is based on results of investigations carried out on porous GaP by means of AFM and STM. Figure 1 shows AFM and STM images on one of porous GaP samples obtained by anodic dissolution of bulk (111)-oriented substrates in H_2SO_4 solutions [4]. The obtained results were compared with SEM images.



(a) (b)

Fig. 1. AFM (a) and STM (b) topographs of the pororus GaP (111) covered with Pt film (1.5 nm)

Surface morphology of the porous matter was acknowledged to be very complicated. Dimensions of porous features vary from quantum size to hundreds nanometers. Their shape has also lots of different modifications. This makes all imaging techniques, including highly resolution techniques, very complicated. Investigated samples contained relatively large structures. However, some undesirable effects were observed by both AFM and STM.

The most crucial of them is the effect of the tip shape [5]. Three concrete situations can appear here. The first is the case when the tip is much smaller than the pores. Subsequently the rendered shape of the feature is much likely to correspond to the true shape and dimensions of the surface morphology. However, the tip and surface damage are very possible in this case. In order to avoid the damage of the tip and the surface of a porous sample two important measures are to be taken. First of all, the pitted porous surface has to be etched in a polishing solution in order to provide a mirror-like surface. In the case of the STM probe relatively high separations between the tip and the surface have to be provided. AFM is desirable to perform in the non-contact mode.

In the case of the tip dimensions being much larger than the mean size of the pores, the imaged shape will correspond more closely to that of the end of the tip. It means that the hillocks of the porous surface scan and image the tip. Such an effect was reported for AFM and analysed by using spectral methods [6]. If the size of the tip is comparable to that of the pores, then the tip fails to penetrate into the finer features of the surface.

This results in the underestimation of the porous degree and morphology. Besides that, the imaged structures do not correspond to the critical size of the porous features. The maximum difference between them can be estimated as it described in Ref. [7]. For the conic tip the maximum error due to the tip size effect corresponds to the diameter of the tip end.

The main purpose and simultaneously the main advantage of the AFM probe is not conductive principle of operation. The permits enables one to use various kinds of materials. No modifications are induced by electrical effects. Another advantage is the predictable shape and size of the scanning tips due to their industrial preparation. These parameters can be used in estimation of the mistake induced by the tip size effect described above. However, this probe possesses a few features that prevent real imaging. One of them is the triangle prism tips which show structures with angles not characteristic for the features of the surface. In order to prevent this effect conic tips are produced. However, the angle of the top of the cone is relatively large in order to prevent fast tip damage. This leads to a not precise imaging.

The tunneling character of the STM probe confirmed the natural passivation of the porous surface in the air. However, the porous matter was shown to keep its conductive character under the vacuum conditions. Therefore, the vacuum is one of the solution which provides the STM functioning on the porous matter. Another solution of escaping the natural passivation is to deposit a metal film on the porous surface. This is also interesting from the point of view of contacts metal-semiconductor. STM measurements in the present work were carried out on porous GaP layers covered with Au or Pt films. The metal films were deposited by thermal and e-beam evaporation. One of the important advantages of the STM set-up used in the present work is the highly sharp tips. They were prepared with simple electropolishing method, according to the necessity, before each STM experiment. It permitted to produce sharp conic tips with varying diameter of the end of the tip. This allowed the imaging with different tip size.

An important effect appears to be characteristic only to the STM probe due to its conductive character. This is the so called "lateral effect". It consists in appearing of the tunneling current on the laterals of the tip while scanning the walls of the porous structure. In the case of a smooth surface the tunnel current density at a certain position of the surface has a Gaussian dependence from the lateral resolution having its maximum at the edge of the tip. While scanning an edge of a surface feature the tunnel current density loses the Gaussian form getting a much complicated one, spreading over a larger part of one or both laterals of the tip. The value of the current remains to be at the same value for a different position of the tip. The result is the bigger microcrystal and smaller pore dimensions of the image than the real ones. Possible solutions of this situation could be digital processing or scanning at a higher scale.

Finally, one can conclude the importance of combination of different imaging techniques. Measurements with different tips and at different scales are also very important measures to obtain successful imaging on a porous material. Experimental results have to be analysed and modelled and compared with other techniques, including non-imaging ones.

This work was supported by the Volkswagen Foundation. I.M.T. acknowledges the support of the Alexander von Humboldt Stiftung.

References

1. L.T. Canham. Silicon quantum wire array fabrication by electrochemical and chemical dissolution of wafers. *Appl. Phys. Lett.* **57** (10), pp. 1046-48 (1990)
2. C.-H. Lin, S.-C. Lee, and Y.-F. Chen. Morphologies and photoluminescence of porous silicon under different etching and oxidation conditions. *J. Appl. Phys.* **75** (12), pp. 7728-36 (1994)
3. B.H. Erné, D. Vanmaekelbergh, and J.J. Kelly. Morphology and strongly enhanced photoresponse of GaP electrodes made porous by anodic etching. *J. Electrochem. Soc.* **143** (1), pp. 305-314 (1996)
4. I.M. Tiginyanu, C. Schwab, J.-J. Grob, B. Prévot, H.L. Hartnagel, A. Vogt, G. Irmer, and J. Monecke. Ion implantation as a tool for controlling the morphology of porous gallium phosphide. *Appl. Phys. Lett.* **71** (26), pp. 3829-31 (1997)
5. K.L. Westra and D.J. Thomson. Effect of tip shape on surface roughness measurements from atomic force microscopy images of thin films. *J. Vac. Sci. Technol. B* **13** (2), pp. 344-349 (1995)
6. S. J. Fang, S. Haplepete, W. Chen, and C.R. Helms. Analyzing atomic force microscopy images using spectral methods. *J. Appl. Phys.* 82 (12), pp. 5891-98 (1997)
7. M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, and K. Murase. Metrology of Atomic Force Microscopy for Si Nano-Structures. *Jpn. J. Appl. Phys.* **34**, pp. 3382-87 (1995)

PLASMA ENHANCED CHEMICAL VAPOUR DEPOSITION OF TUNGSTEN SILICIDE THIN FILMS ON GaAs

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ABSTRACT

Refractory silicides have recently attracted much interest as a possible alternative to polysilicon in interconnect technology and in the development of self-aligned gate technology for Gallium Arsenide field effect devices. The high temperature post anneal step following ion implantation is well suited to the refractory metals and good thermal stability is obtained particularly with the refractory silicides.

Chemical vapour deposition (CVD) of the refractory silicides has largely been used to overcome the deficiencies of sputtering or e-beam deposition, resulting in improved step coverage, adhesion and reduced substrate damage and particle generation. Notwithstanding, the high temperature associated with the CVD process may be reduced and thereby made suitable for GaAs surfaces by the alternative process of Plasma Enhanced Chemical Vapour Deposition (PECVD).

This paper therefore describes the PECVD of tungsten silicide films onto GaAs substrates employing tungsten hexafluoride and silane and the effects of plasma pressure, temperature, gas flow and power on the deposition rate are presented. Further results obtained of physical characteristics, morphology, film integrity, stoichiometry, adhesion and thermal stability are correlated with electrical measurements of sheet resistance, I-V and C-V.

Some preliminary results of a parallel study of PECVD tungsten carbide will also be presented.

Session 4: Heterojunction Bipolar Transistors

14: 00	**Advanced GaAs HBT Power Amplifiers for Novel Applications** *T. Henderson,* D. Hill, M. Tutt, R. Yarborough Triquint Semiconductor Texas, Dallas, Tx	*Invited* USA
14: 30	**Power Amplification Using NPN and PNP HBTs and Application to Push-Pull Circuits** D. Sawdai, *D. Pavlidis* University of Michigan, Ann Arbor, Mi	 USA
14: 40	**Self Aligned Dry Etched Base Emitter and Ledge Technology** *W. John,* H. Wittrich, Herrfurth, P. Wolter, L. Weixelbaum, J. Würfl Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin	 Germany
14: 50	**Novel Coplanar HBT Emitter Design Enabling Fast Fabrication in Two Mesa and Two Metallization Steps** U. Auer, S.-O. Kim, M. Agethen, P. Velling, W. Prost, F.J. Tegude Gerhard-Mercator-Universität Duisburg, Germany:	
15: 00	**Very High Performance InP/ graded-InGaAs/InGaAsP-InP Double Heterojunction DHBT´s for Digital Circuits Operating at 40 Gb/s** *J. Mba,* A.M. Duchenois, P. Berdaguer, J.L. Benchimol, M. Riet France Telekom CNET, Bagneux	 France
15: 10	**Simulation of Influence of Heat Removal on Power Gains of Heterojunction Bipolar Transistors** *R. Stenzel,* J. Würfl, E. Richter, C. Pigorsch, W. Klix Hochschule für Technik und Wirtschaft Dresden	 Germany
15: 20	**Isothermal Characterization of AlGaAs/GaAs Heterojunction Bipolar Transistors for Accurate DC Parameter Extraction** T.C. Kleckner, A.R. St. Denis, *M.K. Jackson* University of British Columbia, Vancouver	 Canada

Advanced GaAs HBT Power Amplifiers for Novel Applications

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The GaAs-based HBT has emerged recently as a commercially viable device for a number of applications. This is due to some of the unique properties of the HBT. For example, the HBT exhibits higher linearity than GaAs-based FETs, with higher gain than Si bipolars. This feature makes the HBT ideally suited for digital modulation and multi-channel communications architectures. Additionally, the HBT also exhibits higher efficiency at low voltages (<3 V) than FETs, resulting in longer talk time in 3 V cellular handset applications. Further, unlike GaAs FET devices, the HBT does not require a negative voltage power supply, saving both die size and complexity.

While the HBT is gaining wide acceptance in the cellular handset market because of the above qualities, there are other attributes that make it ideal for other applications as well. For example, the HBT can exhibit high voltage operation (V_{cc} > 28 V), making HBT a drop-in replacement with greater gain for a wide variety of high voltage L- and S-band Si power devices, such as in cellular phone base stations, cable TV amplifiers, and ground-based radars. Indeed, the this niche market is perhaps the GaAs HBTs best, as many of the high-voltage applications require the high linearity of the HBT as well. In fact, the HBT is the only III-V transistor technology to offer > 15 V operation. We will describe some of the results TriQuint has attained with the high-voltage HBT, and point out some of the unique market applications of the technology. Another niche application is in oscillators, where the HBT has a large advantage due to its low 1/f noise. Finally, HBTs have already demonstrated record power and efficiency numbers from 1-20 GHz.

In this presentation, we will describe a number of the present applications of the HBT, such as in the wireless handset market, and also describe some very promising future applications. The latter include the high voltage microwave amplifier market, high frequency oscillators, and ultra high power amplifiers fabricated through TriQuint's proprietary Low Thermal Impedance (LTI) and Three-Dimensional MIMIC Architecture (3DMA). We will also describe a number of outstanding technical issues, such as optimizing the HBT for linearity and improving HBT device reliability. We will review the key issues in reliability and describe how to simultaneously optimize for reliability and performance. Finally, we will give a brief survey of the different materials technologies (AlGaAs emitter versus GaInP; GaAs-based HBT and InP-based HBT), and new device technologies (GaAs HBT versus SiC and GaN FETs and SiGe HBTs), and describe the current state of the art in HBT performance across the industry.

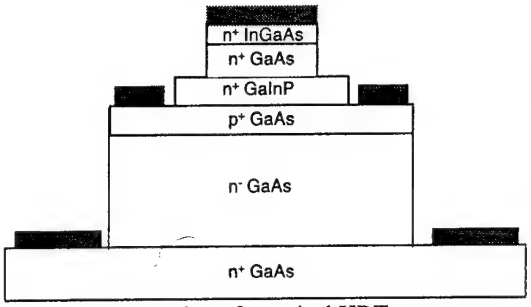


Fig. 1. Cross section of a typical HBT structure

- Low Voltage, high linearity PA's for wireless communications
- High Voltage Amplifiers (CATV, base stations)
- High Power Amplifiers (base stations, T/R Modules)
- Oscillators (C-band and above)

Fig. 2. Applications of HBT Technology

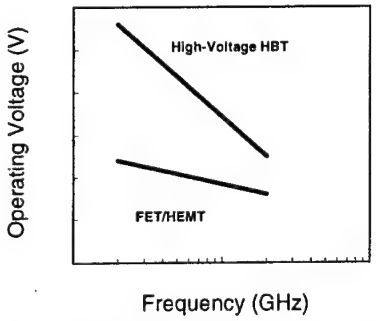


Fig. 3. Schematic of operating voltage versus frequency for GaAs FET and HBT technologies

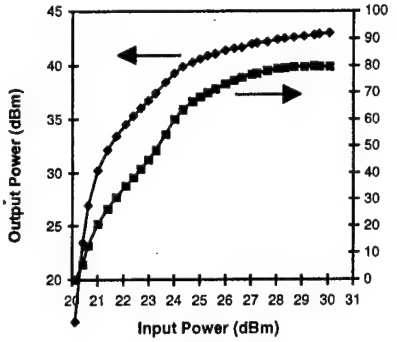
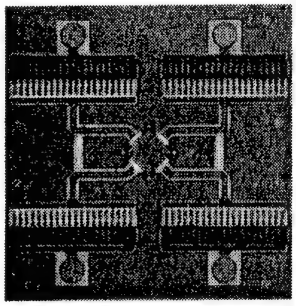
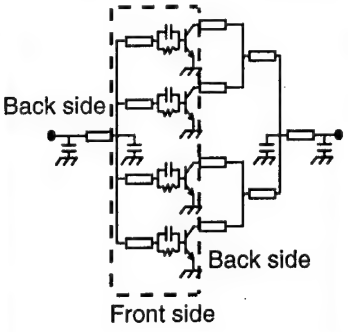


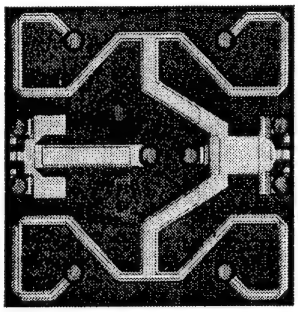
Fig. 4. Power and Power Added Efficiency versus input power for a 2 mm emitter LTI HBT at 1.3 GHz.



Front side of chip



Equivalent circuit



Back side of chip

Fig. 5(a-c). Frontside, backside, and equivalent circuit of a 3DMA high power HBT MMIC amplifier.

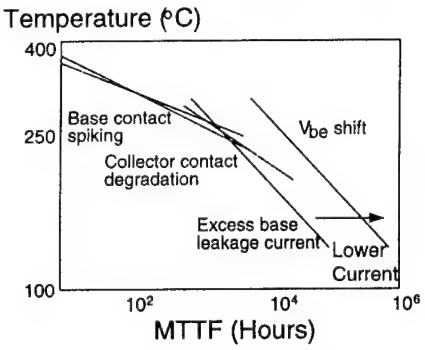


Fig. 6. MTTF as a function of temperature, bias current in an HBT.

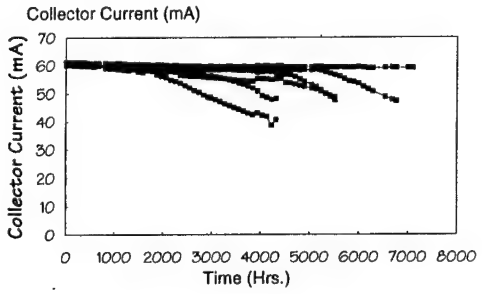


Fig. 7. Collector Current vs. time for a single finger (2x60 μm^2) X-band HBT at T_j = 200 °C.

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Zeuthen, Germany, May 24-27, 1998

Power Amplification using NPN and PNP InP HBTs and Application to Push-Pull Circuits

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InP/InGaAs HBTs have demonstrated very good high-frequency performance and have been implemented in various integrated circuits for electronic and optoelectronic applications. Their power capability is also promising and power levels up to 1.4mW/μm^2 have been reported by the authors using single HBT designs. Their power capability can be enhanced even further by means of double heterojunction designs and a power density of 3.6mW/μm^2 has been reported with the latter approach from Hughes Res. Labs. InP/InGaAs HBTs can consequently be employed in circuits for power amplification. The recent demand for linear power amplifiers prompted the consideration of various approaches for improved performance from existing devices. Various circuit techniques can be used for this purpose and a very promising scheme reported in this paper is the combination of NPN with PNP HBTs in a push-pull amplifier scheme that allows improvement in linearity characteristics.

Unlike NPN HBTs, PNP HBTs have attracted much less attention and little is known about their characteristics, especially under large-signal conditions. The PNP HBTs studied here had a uniformly doped 500Å thick base doped at $5\times10^{18}cm^{-3}$. A self-aligned technology was used for fabrication and Ti/Pt/Au was employed for base metallization. Devices with $5\times10\mu m^2$ emitter fingers showed ideality factors η_B and η_B equal to 1.60 and 1.00 respectively. Their maximum gain at 34kA/cm^2 and V_{CE} equal to 4.0V was greater than 30 while their breakdown was 5.6V. A study of the high frequency characteristics of the devices showed a current gain cutoff frequency of 11GHz and a maximum oscillation frequency of 31GHz. This exceeds the best-reported performance for InAlAs/InGaAs PNP HBTs which was 22GHz. The devices were characterized using load pull techniques and demonstrated a small-signal gain of 10dB, peak power-added-efficiency of 24% and maximum output power density of 0.5mW/μm^2. These characteristics are very similar to NPN InP-based HBTs fabricated with the same technology. The latter devices had slightly higher gain (+1dB) and efficiency (+5%), while the PNP HBTs produced more power (+3dBm).

A push-pull amplifier was studied using the fabricated NPN and PNP HBTs. While for single HBTs class-B operation shows better efficiency but worse linearity, push-pull amplifiers can combine these two features and maintain therefore high linearity and efficiency under class-B conditions. A coplanar circuit was developed to permit feeding of the NPN and PNP HBTs from a common input signal terminal. The devices were thinned to 200μm and mounted on 10mil alumina substrates. Electromechanical tuners were used to increase the PNP gain and match it to that of NPN devices. Testing of the circuit showed best IM3 (by ~7dBc) and small second harmonic content (by ~9dBc) compared with NPN HBTs. Overall, we report the development of PNP and NPN technology and its application to push-pull amplifier circuits with improved power performance.

Work supported by ARO-MURI (DAAH04-96-1-0001)

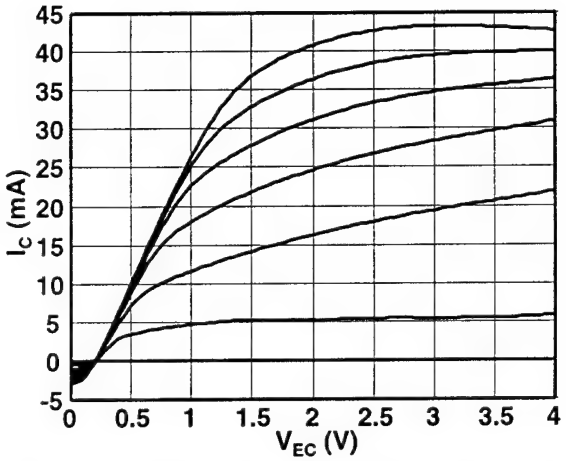

Figure 1: Forward I-V characteristics of 5×10 μm² PNP HBT. I_B = 0.5 mA/step. For this HBT, f_T =11 GHz and f_{max} = 31 GHz at J_C = 23 kA/cm².

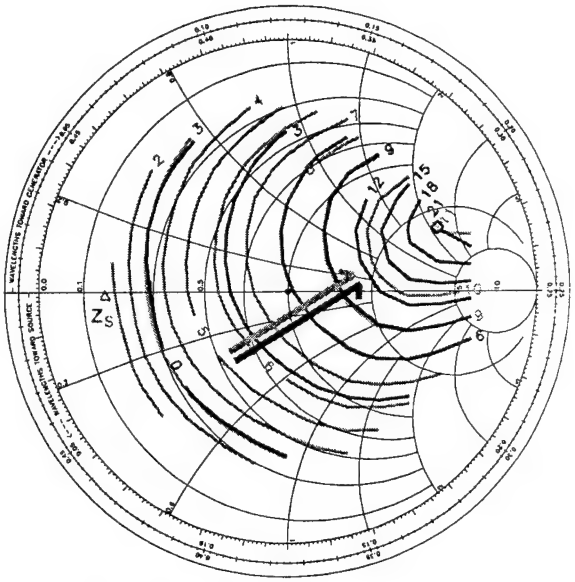

Figure 2: On-wafer load pull at 10 GHz of 5×10 μm² PNP HBT measured at P_{in} = 3.17 dBm under constant V_{EB} bias with V_{EC} = 4.0 V. Both maximum P_{out} = 0.50 mW/μm² and PAE = 24% occur at slightly higher P_{in}.

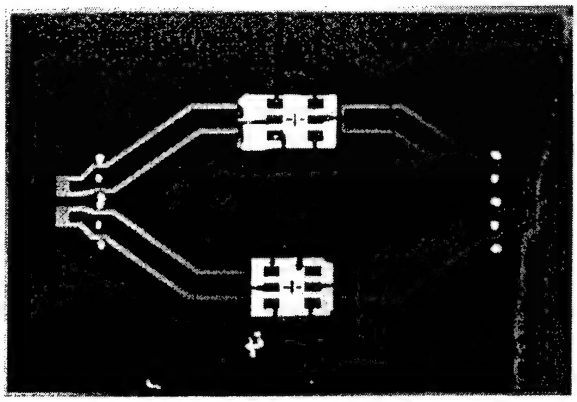

Figure 3: NPN/PNP push-pull common-emitter amplifier. The NPN and PNP HBTs were individually fabricated.

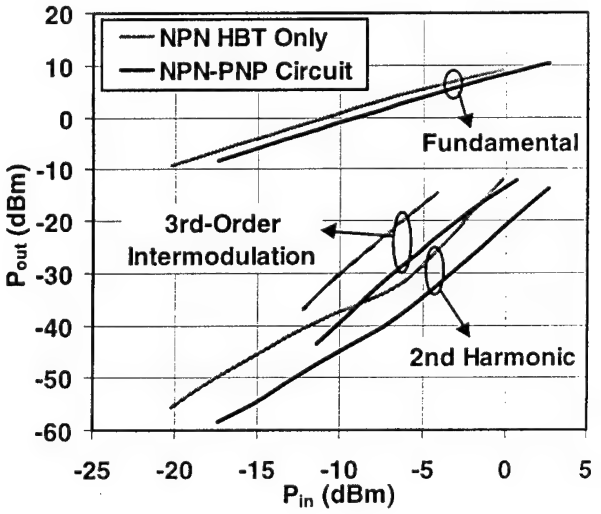

Figure 4: Power characterization of NPN/PNP push-pull common-emitter amplifier at 8 GHz. The 2nd harmonic and 3rd-order intermodulation (500 kHz separation) are improved when compared to a single NPN HBT amplifier.

Self Aligned Ledge Technology for AlGaAs/GaAs Heterojunction Bipolar Transistors

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Abstract

The passivation of the extrinsic base region using a depleted emitter ledge technology significantly reduces surface recombination currents. This results in increased current gain and reduced 1/f noise. The emitter ledge usually consists of a thin, depleted wide gap emitter layer (AlGaAs or InGaP) that passivates the area between the emitter mesa and the base metallization. A reproducible self aligned ledge technology requires well defined emitter geometries. Therefore a material RIE selective dry etch process in combination with a sidewall deposition technique of the ledge and the emitter periphery has been developed.

The HBT structure that has been used for device optimization is given in table 1. The process starts with the deposition of a refractory WSiN layer on top of the InGaAs cap. Afterwards a TiPtAu layer, structurized by liftoff technique, defines the lateral emitter dimensions. The TiPtAu layer serves as a mask for the self aligned emitter and ledge process. Figure 1 represents a schematic cross section of the process. At first, the refractory WSiN-layer is etched in a SF_6 : Ar plasma (225 V; 1 Pa; 50 W). The subsequent InGaAs cap etching is carried out in BCl_3 : Ar ambient at relatively high bias conditions (370 V; 1 Pa, 100 W) to ensure the removal of non volatile Indium chlorides. As soon as the InGaAs layer has been structurized, the SF_6 gas component is added and the plasma parameters are changed towards low bias conditions (25 V; 15 Pa, 30 W). This facilitates a material selective etch stop on top of the AlGaAs wide gap emitter. The degree of minimum mask underetching depends on the over etching time that is necessary to obtain a material selective etch stop. Therefore the surface morphology of the InGaAs cap layer plays a decisive role. For nearly specular InGaAs layers with a roughness below 5 nm the minimum undercut during dry etching can be limited to about 200 nm. Larger undercuts are of course always feasible and depend on the process parameters (e.g. over etch time). After emitter dry etching the complete structure is covered by a 150 nm SiNx passivation layer and is anisotropically structurized in a SF_6: Ar plasma. Thus only the sidewall regions and the regions decorating the emitter undercut are left over (see Figure 1 and 2). A subsequent wet chemical etching of the AlGaAs emitter layer completes the process. During wet chemical AlGaAs removal the sidewall passivation protects the emitter mesa and allows for the ledge definition. Figure 2 shows a REM cross section of a dry etched and side wall passivated emitter structure with a relatively large undercut of more than 500 nm to show process details.

After emitter definition the base contacts are evaporated. The process is completed using standard triple mesa technology in combination with planarization and interconnection layers Figure 3 shows a Gummel Plot of the HBT structures. The current gain of the transistors exceeds 100 and is widely independent on emitter size and emitter periphery.

Material	Doping conc. [cm^{-3}]	Thickness [nm]	Function
InGaAs	$1 * 10^{19}$ (Si)	30	Cap
InGaAs --> GaAs	$1 * 10^{19}$ (Si)	20	Cap grading
GaAs	$4 * 10^{18}$ (Si)	300	GaAs-cap
GaAs --> AlGaAs	$3 * 10^{17}$ (Si)	20	Emitter grading
AlGaAs	$3 * 10^{17}$ (Si)	80	Widegap-emitter
AlGaAs --> GaAs	$3 * 10^{17}$ (Si)	20	Emitter-base grading
GaAs	$4 * 10^{19}$ (C)	100	Base
GaAs	$3 * 10^{16}$ (Si)	500	Collector
GaAs	$4 * 10^{18}$ (Si)	500	Subcollector

Table 1: Epitaxial design of the AlGaAs/GaAs HBTs

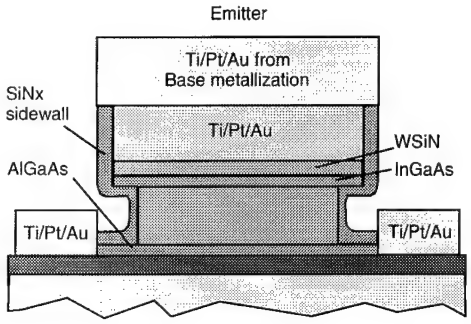

Figure 1: Schematic cross section of the self aligned emitter and ledge technology

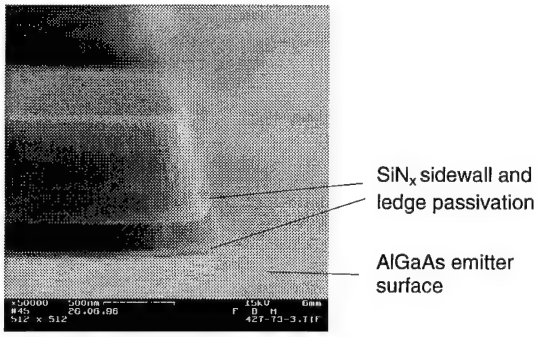

Figure 2: SEM image of a emitter structure showing the SiNx coated AlGaAs ledge after anisotropic back etching

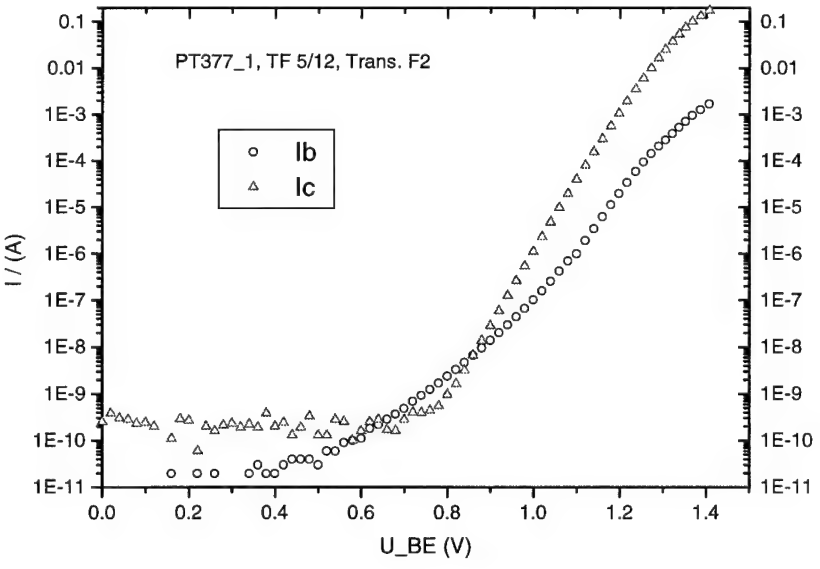

Figure 2: Gummel plot of a typical HBT-structure showing current gain exceeding 100

Novel Coplanar HBT Emitter Design Enabling Fast Fabrication in Two Mesa and Two Metalization Steps

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Abstract

The challenge of Heterostructure Bipolar Transistors (HBT) technology is the realization of both a low emitter and a low base mesa area. Conventionally [e.g. 1], a time consuming and sophisticated technology (three metalization and three mesa steps, air-bridge technology) is a prerequisite to provide high performance devices due to a low base area realization and a low base-collector feedback capacitance.

In this work, we present a novel coplanar Ω-type emitter (E) design with inserted small area T-shaped base (B) contact. The used E-B-E instead of a B-E-B configuration theoretically shows better performance [2]. Furthermore, it enables an easy and very fast 4 step fabrication process using conventional technology based on optical lithography.

The key technology step is the simultaneous and fully self-aligned evaporation of base and collector metalization which is enabled by the new design. This way, the fabrication time in comparison to a conventional process [e.g. 1] is reduced to at least by 1/3 regardless of any plated air-bridge efforts which are not used here. Moreover, the base width is as lower as 0.5 µm resulting in an almost ideal emitter to base mesa area ratio of A_E/A_{Bmesa}= 0.9. In addition, the design simply allows the connection of two emitter contact pads resulting in a direct coplanar device topology without any air-bridge crossing.

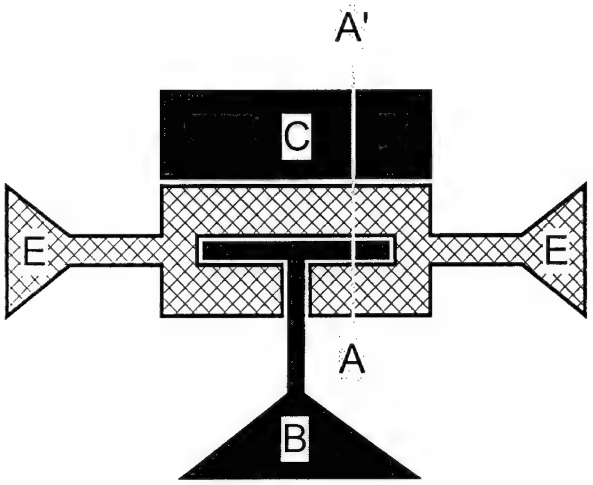
The design is adopted to carbon doped InP/InGaAs HBTs grown by LP-MOVPE resulting in very promising device performance ($f_T \geq$ 100 GHz). Especially, a low feed back (S_{12}<0.1) is measured up to 45 GHz due to the excellent mesa area ratio (A_E/A_{Bmesa}). This feedback value is approximately 1/3 of conventional high performance HBT devices.

In summary, a fast and easy HBT fabrication based on a new Ω-type emitter design is presented exhibiting ultra low feedback. This new technology is suited for a wide variety of materials systems and may contribute to the success of HBTs in high speed circuits due to a low cost fabrication.

References

[1] Yutaka Matsuoka, Shoji Yamahata, Kenji Jurishima and Hiroshi Ito: *„Ultrahigh-Speed InP/InGaAs Double-Heterostructure Bipolar Transistors and Analyses of Their Operation"*, Jpn. J. Appl. Phys. Vol. 35 (1996) pp. 5646-5654

[2] G.-B. Gao, D.J. Roulston, H. Morkoç: *„Design study of AlGaAs/GaAs HBT's"*, IEEE Trans. Electron Devices, Vol. 37, No. 5 (1990) pp. 1199-1207.



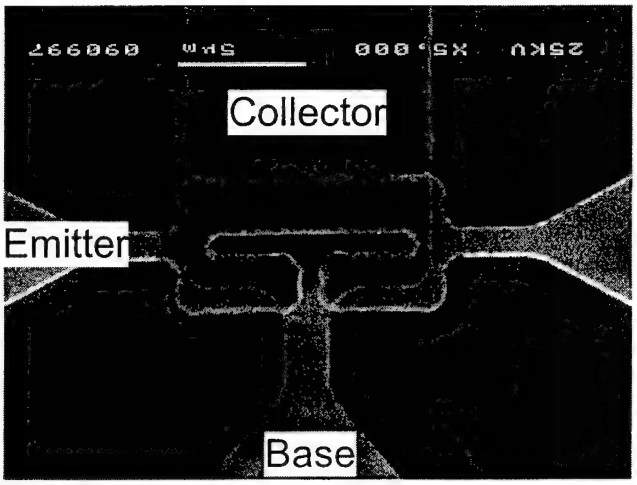


Fig. 1: Ω-shape emitter and T-shape base metal structure (right: SEM-photography of fabricated HBT).

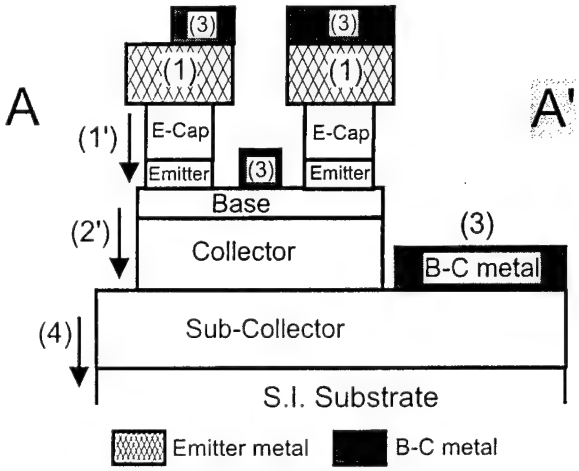


Fig. 2: The cross-section of the fully self-aligned two metalization HBT.

Processing Steps

(1) the *first* metalization (emitter electrode) and etching to base layer

(2) base definition with photoresist and etching to sub-collector layer

(3) the *second* metalization (base and collector electrode)

(4) collector mesa and etching to substrate for mesa isolation

Table 1: Processing steps.

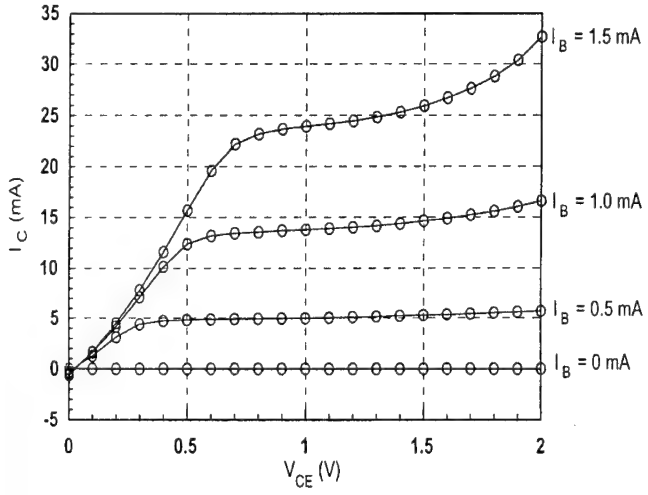


Fig. 3: The common-emitter output characteristics of the InP/InGaAs HBT with spacer layer between emitter and base (N_B =5x10^{18}cm^{-3} ; A_E=40 μm^2).

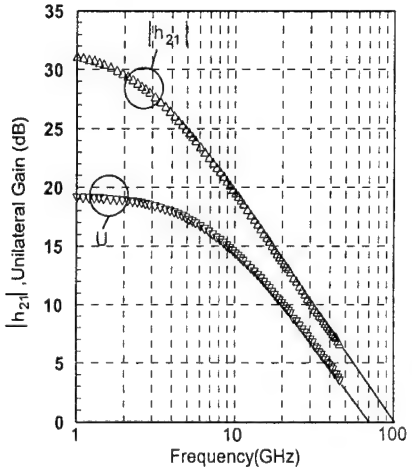


Fig. 4: The extrinsic cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) as measured.

Very High Performance InP/graded-InGaAs /InGaAsP-InP Double Heterojunction DHBT's for digital circuits operating at 40Gb/s.

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The rapid development of high-speed digital and microwave applications has created a need for very high performance devices. Recently, the Double Heterojunction Bipolar Transistor (DHBT) in the InP/GaInAs/GaInAsP-InP material system has been used to fabricate circuits operating at 20Gb/s and above, such as selector, decision circuit and demultiplexer [1]. Those DHBT present the following performances : cutoff frequencies F_t = 55GHz, F_{max} = 45GHz, a static gain of 60, breakdown voltage BVce = 12.5V. To fabricate circuits operating at 40Gb/s, transistors with F_t > 80GHz and F_{max} >60GHz are needed without decreasing the static gain (50) or BVce (8V). The high dynamic and static DHBT performances depend directly on base-collector junction. In this paper, we discuss the two ways for optimizing DHBT performances : optimization of base characteristics (doping level, thickness and composition); the reduction of both the active area and the thickness of the base-collector.

•***HBT epitaxial structure and technology***. The epitaxial structure, grown by Chemical Beam Epitaxy (CBE), is shown on figure 1 : the double heterojunction leads to a large BVce (14V). The presence of GaInAs spacer and GaInAsP quaternary layers helps improving the current collection. The emitter, base and collector mesas are achieved by a combination of wet and ion beam etching. The n and p ohmic contacts are realized with Ti (200Å)/Pt (300Å)/Au (2500Å) and annealed at 300°C[2].

•***Optimization of base characteristics : doping level (N_B), thickness (W_B) and composition***. To increase the cutoff frequency Ft and static gain of the DHBT, one has to decrease the transit time of electron in the base τ_B ($\tau_B = \frac{W_B^2}{2D_{nB}}$; where D_{nB} is the diffusion coefficient of the electron in the base), and to minimize the possibilities of recombination in the base[3]. Both requirements call for a thin base layer as shown on figures 2 and 3. Nevertheless, an immediate consequence of a reduction of the base thickness is the increase of R_{car} ($R_{car} = \frac{2{,}51.10^{14}}{W_B . N_B^{0.865}}$) (figure 3) and therefore a decrease of F_{max}. To go through this last difficulty, it is necessary to have a high doping level in the base which implies a reduction of the current gain. In the light of this analysis, it seems very important to find a tradeoff between the reduction of W_B and the increase of N_B. The tradeoff used in our work is to design a DHBT with a carbon doped ***graded base*** [4]: $Ga_{1-x}In_xAs$ ($0.53 \leq x \leq 0.46$). This permits to increase the electric field in the base and thus to obtain a high current gain although the base has large doping level and thickness (figure 4). Experiments with base parameters (W_B = 600Å and $N_B = 7.10^{19}cm^{-3}$), give a gain of 46 with R_{car} = 380Ω/□ for the graded base, while the gain = 2 for non-graded base.

•***Reduction of mesa base area (S_{bc})*** in order to reduce the base-collector capacitance (C_{BC}) and then to have better cutoff frequencies (Ft and Fmax). Since it is not possible to turn GaInAs to semi-insulating by ion implantation, the base-collector area is reduced by etching part of the base mesa and replacing it by an insulating material (polyimide). This permits to lay part of the base contact on polyimide (figures 5 and 6). With this technology, the base-collector area was reduced by a factor of 30% to 51% depending on the DHBT geometry. As examples, we obtained C_{BC}=71fF, f_t=56GHz and f_{max} = 42GHz for S_{BC} = 166μm² versus C_{BC} = 37fF, f_t=71GHz et f_{max}= 53GHz with the reduced S_{BC} (90μm²).

•***Optimization of collector :*** to reduce the transit time of electrons in the collector, it is necessary to have a thin collector layer. However, since this results in a large base-collector capacitance detrimental to the obtention of high performances, an over-etch of the collector mesa is mandatory. To decrease the InP collector area (40%) and thus to keep a small C_{BC}, we have to further reduce S_{BC} by making an over-etching of the InP collector (20 à 30%). Many experiments have shown that this approach can be used for a collector thickness of about 2500Å - 3500Å.

DHBT structures benefiting simultaneously from the graded base (carbon $810^{19}cm^{-3}$, 600Å), thin collector (2500Å), capacitance reduction technology and collector over-etching lead to : F_t = 103GHz, F_{max} = 65GHz, gain = 46, BVce = 8.5V at 1.6V and 40000A/cm² for DHBT with S_{eb} = 11*4μm² (figure 7).

DHBT STRUCTURE

Layer		Material	Doping	Thickness
Emitter Contact		InGaAs InP	Si 2E19 Si 2E19	110 nm 60 nm
Emitter		InP	Si 2E17	150 nm
Base		InGaAs	C 3E19	55 nm
Collector	C1	InGaAs	Si 2E16	20 nm
	C2	InAGaAsP (Eg = 0,95 eV)	Si 5E16	20 nm
	C3	InGaAsP (Eg = 1,15 eV)	Si 5E16	20 nm
	C4	InP	Si 2E16	520 nm
Collector Contact		InP InGaAs InP	Si 2E19 Si 2E19 Si 2E19	55 nm 220 nm 320 nm
S.I Substrate : InP				

Figure : 1

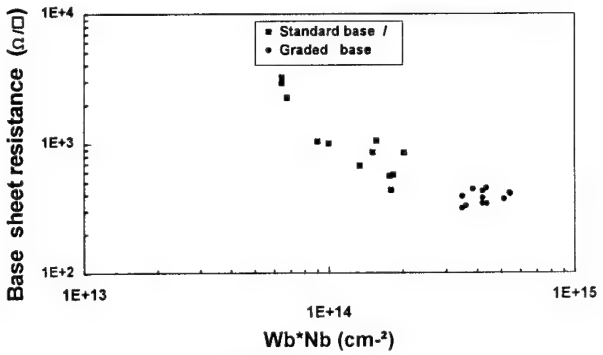

Figure 2

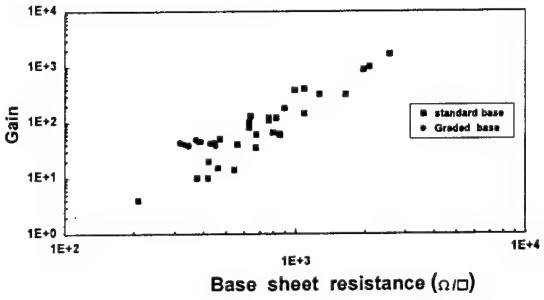

Figure 3

DHBT STRUCTURE : graded-base and thin collector

Layer		Material	Doping	Thickness
Emitter Contact		GaInAs InP	Si 2E19 Si 2E19	110 nm 60 nm
Emitter		InP	Si 2E17	150 nm
Base		*graded-InGaAs*	*C 7E19*	*60 nm*
Collector	C1	InGaAs	Si 2E16	20 nm
	C2	InGaAsP (Eg = 0,95 eV)	Si 5E16	20 nm
	C3	InGaAsP (Eg = 1,15 eV)	Si 5E16	20 nm
	C4	InP	Si 2E16	*250 nm*
Collector Contact		InP InGaAs InP	Si 2E19 Si 2E19 Si 2E19	55 nm 220 nm 320 nm
S.I Substrate : InP				

Figure : 4

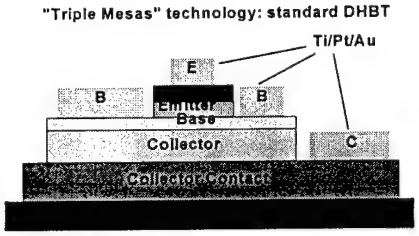

Figure 5

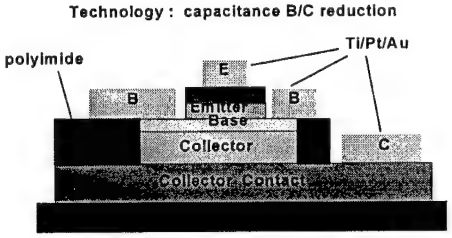

Figure 6

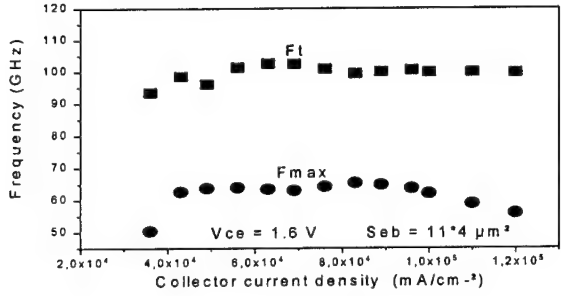

Figure 7

Bibliography

[1] J. Godin, P. André, P. Desrousseaux, A.M. Duchenois, A. Konczykowska, and al : "A InP DHBT technology for High Bit-rate Optical Communications Circuits" GaAs IC Symposium pp.219 - 222 (Oct 1997).

[2] D. Caffin, M. Bouché, M. Meghelli, A.M. Duchenois, and P. Launay, "InGaAs/InP double-HBT technology for high bit rate communication circuits". Electronics Letters pp. 149-151 Vol.33 No.2 (Jan 1996).

[3] R.N. Nottenburg, H. Temkin, M.B. Panish, R. Bhat and J.C. Bischoff : "InP/GaInAS double-heterostructure bipolar transistors with near-ideal β versus Ic characteristic" IEEE Electron Devices Lett., vol. EDL-7, no. 11, p. 643, 1986.

[4] J.L. Benchimol, J. Mba, B. Sermage and al: "CBE growth of carbon doped InGaAs/InP HBT's for 25 Gbit/s circuits". Submitted for publication to J. Crystal Grow (Dec. 1997).

SIMULATION OF INFLUENCE OF HEAT REMOVAL ON POWER GAINS OF HETEROJUNCTION BIPOLAR TRANSISTORS

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Abstract

Heat removal from heterojunction bipolar transistors (HBT) during power operation is an important assumption to improve gains and reliability. For an analysis of the influence of different thermal boundary conditions numerical simulations of HBT structures have been carried out.

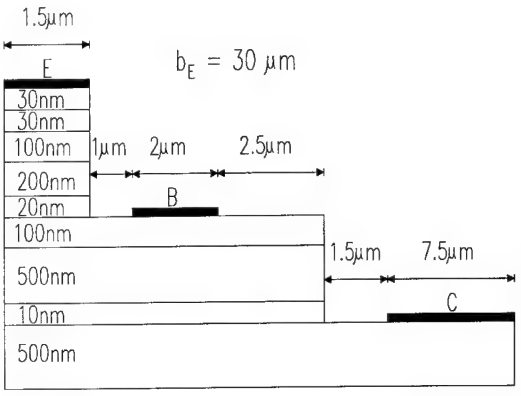
For the modeling of the HBT we used our 2D/3D program SIMBA [1,2], which is based on a self-consistent solution of a drift-diffusion model coupled with the heat flow equation to include non-uniform lattice temperatures. Thermal boundary conditions can be ideal thermal contacts, ideal thermal isolation and radiation thermal boundary conditions, which are determined by a surface thermal conductivity and a reference temperature.

Fig. 1 shows the basic GaInP/GaAs-HBT structure and the layer parameters used for the simulations. At the bottom an additional 20 µm undoped substrate part and a thermal conductivity of 20 W/cmK, which corresponds to a wafer thickness of 500 µm, was considered. At the emitter contact we assumed a thermal conductivity of 5000 W/cmK and at base and collector contacts a 10 times smaller value. Between the contacts a thermal conductivity of 50 W/cmK was fixed. The calculated temperature distribution at a high current density of $2 \cdot 10^5$ A/cm^2 (V_{CE} = 3V) is represented in Fig. 2. The Maximum of temperature is about 435 K within the collector area. The corresponding cut-off frequencies f_{max} and f_t as a function of collector current are shown in Fig. 3 (solid line). A strong drop appears at a collector current density of about $4 \cdot 10^4$ A/cm^2 due to the increase heating-up. One approach to avoid this could be a better heat removal caused by an overlap of the emitter contact metal, which is insulated by Si_3N_4. The resulting efficiency at a thermal conductivity of 5000 W/cmK is also shown in Fig. 3 (dashed line). The maximum of cut-off frequencies can be obtained up to a current density of about $1 \cdot 10^5$ A/cm^2. In comparison the results for a narrower emitter at the same area and conventional contacts are depicted.

For a verification of the thermal model experimental results of a conventional structure have been compared with simulation results.

[1] R. Stenzel, W. Klix, R. Dittmann, C. Pigorsch, F. Schnieder:
Numerical simulation of III/V-semiconductor devices with SIMBA.
Proc. of 8th GaAs Simulation Workshop, Duisburg 1994, pp. 1-35

[2] W. Klix, R. Dittmann, R. Stenzel:
Three-dimensional simulation of semiconductor devices.
Lecture Notes in Computer Science 796, Springer-Verlag, 1994, pp. 99-104



Material	Thickness	Doping
InGaAs	30 nm	$1 \cdot 10^{19}$ cm^{-3}
InGaAs...GaAs	30 nm	$1 \cdot 10^{19}$ cm^{-3}
GaAs	100 nm	$4 \cdot 10^{18}$ cm^{-3}
GaAs	200 nm	$4 \cdot 10^{17}$ cm^{-3}
InGaP	20 nm	$1 \cdot 10^{17}$ cm^{-3}
GaAs	100 nm	$4 \cdot 10^{19}$ cm^{-3} (p)
GaAs	500 nm	$3 \cdot 10^{16}$ cm^{-3}
InGaP	10 nm	$4 \cdot 10^{18}$ cm^{-3}
GaAs	500 nm	$4 \cdot 10^{18}$ cm^{-3}

Fig. 1: HBT structure and layer parameters

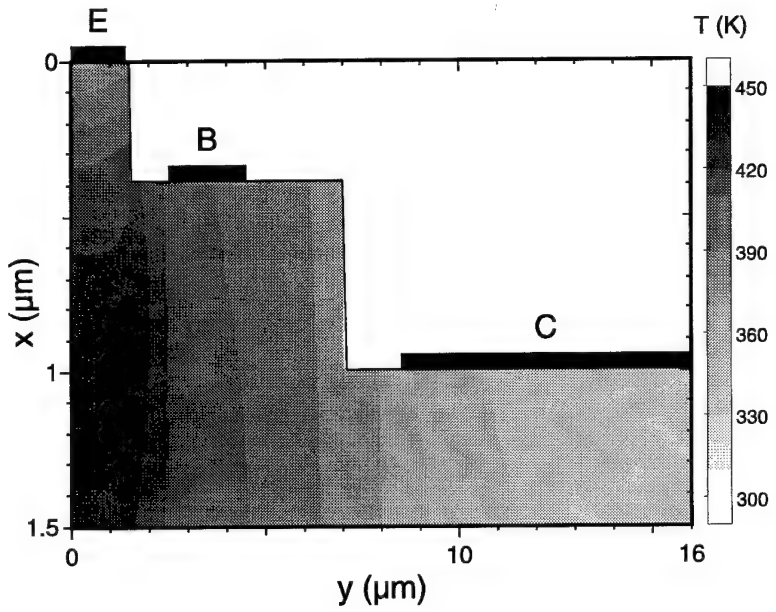


Fig. 2: Temperature distribution at V_{CE} = 3 V and $J_C = 2 \cdot 10^5$ A/cm^2

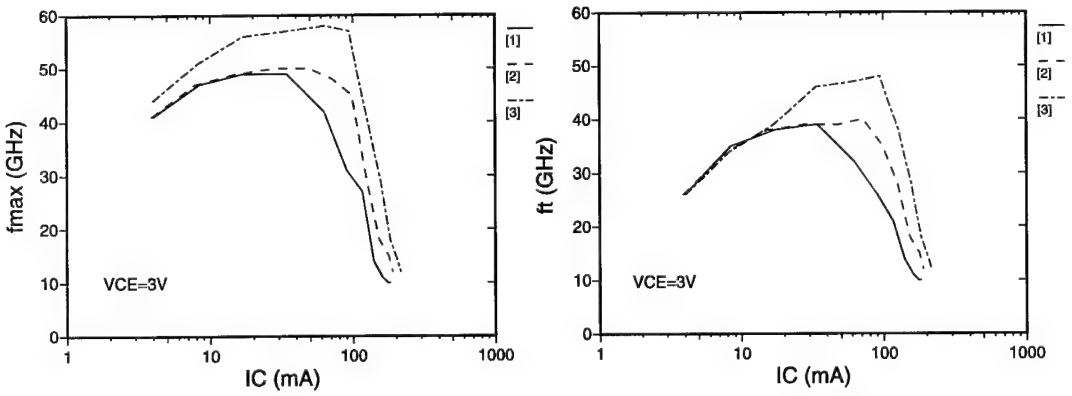


Fig. 3: f_{max} and f_t versus collector current ([1]: basic structure, [2]: improved thermal surface conductivity between emitter and base contact, [3]: emitter area 2x45 µm^2)

Isothermal Characterization of AlGaAs/GaAs Heterojunction Bipolar Transistors for Accurate DC Parameter Extraction

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Extraction of compact model parameters is a crucial issue in high-performance circuit design as accurate parameters are required for reliable circuit simulation. Typically DC parameters are extracted by applying a variety of biases to the device under test, maintaining the substrate temperature constant. However, the non-zero device power dissipation results in self-heating. This causes errors as the device temperature is varying and not equal to the substrate temperature. Circuit simulation errors will be greatest when the operating conditions differ substantially from those for characterization, and is particularly pronounced in large-signal switching. In this paper we describe a new technique to perform isothermal device characterization.

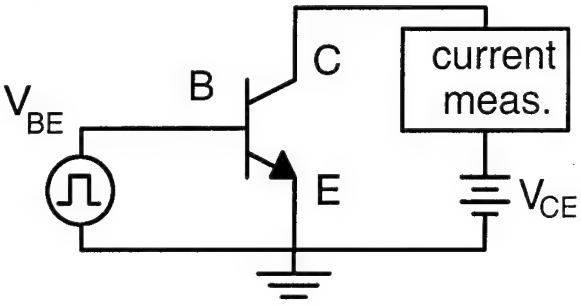

Figure 1 – Schematic experimental setup.

In Fig. 1 we show the experimental setup. A pulsed base bias is applied to switch from an initial state where power dissipation is negligible to a final state in which the dissipation is high; finally the base bias is returned to the initial level. Two steps are taken to ensure that the initial device temperature is equal to that of the substrate. First, we choose a 1% duty cycle so that self-heating from the previous pulse is negligible. Second, we ensure that the power dissipation in the initial state is significantly lower than in the final state by using an initial base bias 200mV below the final level. A rise time of 150ns is used, and measurements were performed at 296K. The collector voltage is maintained constant, and the collector current is monitored with a digital oscilloscope. The device studied in the present work is an AlGaAs/GaAs heterojunction bipolar transistor with a 3x3μm emitter. Further details of device fabrication are given in [1].

In Fig. 2 we show the collector current waveforms for two base biases as solid lines; the collector bias is 3.0V. In both cases the collector current rises rapidly as the base bias rises; this is followed by a slower rise to the steady-state value as the device temperature rises. In the lower curve the degree of self-heating is small, so the the difference between initial and final currents is small. In the upper curve the power dissipation is higher, resulting in greater self-heating as evidenced by the more pronounced increase of collector current during self-heating. We fit an exponential function to the collector current transients for the period over which the base bias is constant. In Fig. 2 we show these fits with dashed lines. For the lower curve the fit is excellent, and the thermal time constant is 1.8μs. We note that the thermal response is well described by a single time constant, even though other authors have argued that several time constants could play significant roles because of the three-dimensional heat flow [2]. The quality of fit for the upper curve is poor: there are two possible reasons for this. The first is that the thermal conductivity changes substantially as the temperature rises. The second, and we believe the dominant cause, is the presence of pronounced electrothermal

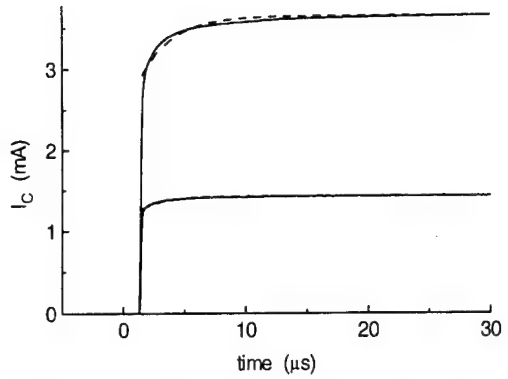

Figure 2 – Collector current transients for base biases of 1.390 and 1.425V. The solid lines show experimental results, and the dashed lines the fit.

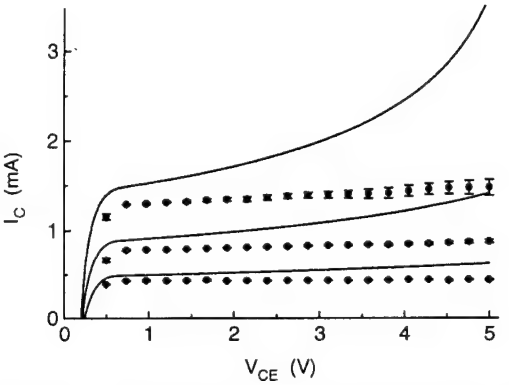

Figure 3 – Isothermal (symbols) and steady-state (solid lines) collector characteristics for base-emitter biases of 1.351, 1.371 and 1.390V.

feedback for higher levels of power dissipation. Increasing device temperature during the transient results in further increases in collector current because the built-in potential of the base-emitter junction decreases with increasing temperature [3].

We now discuss the method to extract the isothermal device response. As the base rise time is an order of magnitude less than the thermal time constant, little self-heating occurs during the rise time. Therefore, once the base bias has risen, the device temperature is still very close to the substrate temperature. We can extrapolate the leading edge of the collector current transient to the time where the base pulse bias was initially applied, and estimate the collector current for the device at the ambient temperature; this is what we refer to as the

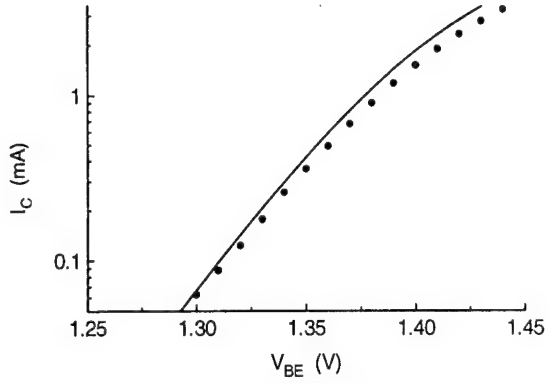

Figure 4 – Gummel plot showing isothermal (symbols) and steady-state (solid line) collector current.

"isothermal" response. In Fig. 3 the symbols show the isothermal collector characteristics for three base voltages. For comparison we show the steady-state collector characteristics with the solid lines. The discrepancies between the isothermal and steady-state curves are substantial. This indicates that while parameter extraction of quantities such as the Early voltage, for example, are impossible using steady state measurements, such extractions can easily be performed with data such as that shown in Fig. 3.

Another important form of data for parameter extraction is the Gummel plot, shown in Fig. 4. The symbols show the isothermal collector current, and the solid line shows the steady state collector current. Significant discrepancies are seen between the two curves. The isothermal knee current I_K, which models β_F rolloff due to high current effects, is overestimated if extracted from the steady-state Gummel plot. The origin of the effect is again seen by considering the increase of I_C for increasing temperatures; the tendency of device parasitics r_b and r_e to debias the base-emitter junction at high currents is countered by the larger collector currents arising from the larger corresponding power dissipation and junction temperature.

The authors would like to acknowledge Nortel Technology for supplying the devices tested, NSERC Strategic Grants. One of us (TCK) acknowledges NSERC and BC ASI fellowship support.

[1] T. Lester et al., Proc. 20th Int. Sy. GaAs Related Compounds, 1993.
[2] W. Liu, Jpn. J. Appl. Phys. **32**, 5503(1993).
[3] Q. M. Zhang et al., IEEE MTT, Vol. 44, No. **11**, 2001(1996).

Session 5: Field Effect Transistors

15: 30 **Reliable Complementary HIGFET Technology for High Speed/Low Power Applications**
M. Touirat, M., Roger, H. Fawaz, J.-F. Thiey, N. Linh, E. Delos, G. Salmer
IEMN, Villeneuve **France**

15: 40 **Optical Effects in p-Channel InGaP/GaAs/InGaAs Double Heterojunction Pseudomorphic MODFET**
H.J. Kim, D. M. Kim, J. I. Lee, J. Zimmermann
Korea Institute of Science and Technology, Seoul Korea

15: 50 **First Low Temperature Grown InP-channel HFET on GaAs Substrate**
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University of Ulm Germany

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Russian Academy of Sciences, Chernogolovka Russia

RELIABLE COMPLEMENTARY HIGFET TECHNOLOGY FOR HIGH SPEED/LOW POWER APPLICATIONS

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Recently, low voltage operation very high speed transistors with ultra-low power dissipation are strongly required in developing advanced high performance integrated circuits for portable systems. Pseudomorphic AlGaAs/InGaAs/GaAs Heterostructure Insulator Gate Field-Effect-Transistors (HIGFET's) are attractive devices in the application to high speed/low power IC's due to their potential advantages over Si CMOS circuits of equivalent gate dimensions, i.e., superior speed performance, lower threshold voltage sensitivity, constant speed versus temperature, and process simplicity. A complementary HIGFET (C-HIGFET) process has been developed in IEMN intended for high speed/low power digital IC's. In this paper, we present the C-HIGFET process and device results. Also, this presentation discusses short channel effects in submicron N and P-channel transistors.

The HIGFET device structure is shown in Fig. 1. A schematic cross-section of the self-aligned ion-implantated C-HIGFET process is shown on Fig.2. The gate metal was RF sputtered WSi (4000 Å) with a nominal gate length ranging from 1µm to 0.3µm. N-channel (Si) and P-channel (Be + P co-implant) source/drain implants were self aligned to the gate. AuGe/Ni/Au and Au/Mn/Ni/Au ohmic contacts are then defined for N-channel and P-channel devices respectively. The interconnect metallisations were Ti/Au. Devices are finally passivated with Si_3N_4.

Typical I-V characteristics of $2*20*1\mu m^2$ N and P-channel are shown in Fig. 3 and 4. The threshold voltage are near 0.55V for N-HIGFET and -0.4V for P-HIGFET. The device has very good pinch-off characteristics and output conductance. Typical device parameters are given in Table 1. The P-channel transistor demonstrated a transconductance of 65 mS/mm and a turn-on voltage, defined as the gate voltage resulting in $1\mu A/\mu m^2$ gate current at Vds=0, is -2.2V. These performances are superior to previous P-channel HIGFET of similar dimensions even reported. The N-channel HIGFET correspondingly shows a turn-on voltage of 1.4V.

The standard deviation of the 1µm device threshold voltage over 2-inch wafers was 35mV for the N-HIGFET and 26mV for the P-HIGFET respectively. The distribution of the threshold voltage of both N and P-type transistors is reported on Fig. 5 and 6. Concerning the process yield, a mean value of 90% was obtained, with a maximum occurrence of 99% for the best wafer. Histograms of the measured drain current Ids at Vgs=2V are shown on Fig. 7 and 8.

Furthermore, submicron devices have been fabricated using the same process. The results clearly show that short-channel effects arise below 0.7µm channel length, with an important shift of the threshold voltage for 0.3µm devices (Fig. 9). This is due to the implanted straggle effects, which can be minimised by using sidewalls (Fig. 9, solid line curve). The SiO_2 sidewall structure we used is represented on Fig. 10. Typical N-HIGFET performances are given in Table 2 and compared to conventional N-type device's (Table 1): Quasi-similar characteristics are obtained for long-channel devices (Lg=1µm) but much better ones are performed for 0.3µm transistors (especially the threshold voltage and the subthreshold current).

In a close future, the sidewall process will be optimised for P-type channels in order to assess the complementary submicron HIGFET technology.

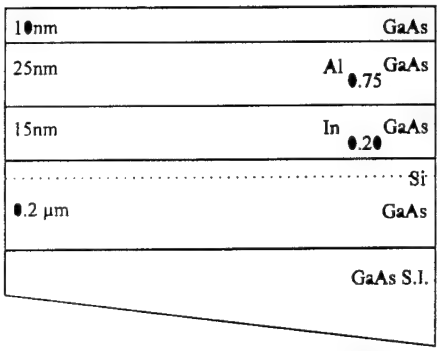

Fig. 1 : Cross-section of HIGFET epitaxy

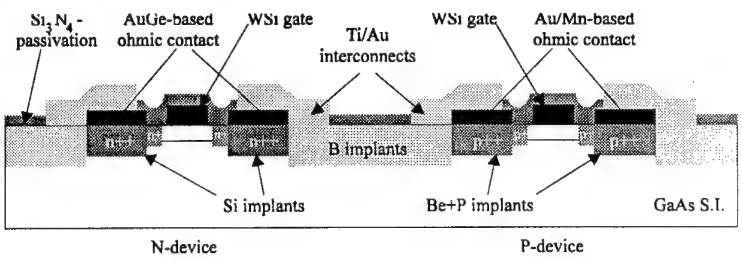

Fig. 2 : Complementary HIGFET technology

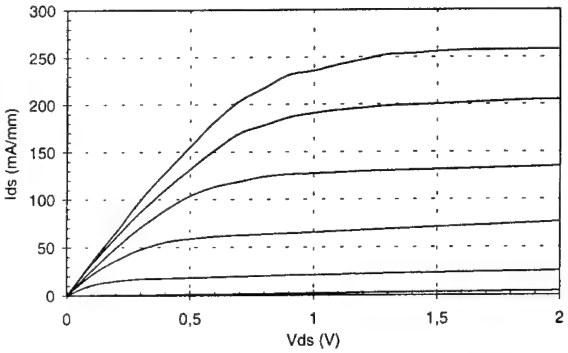

Fig. 3 : I-V measurement of 1µm-N-HIGFET. Vgs max = 1.6 V. Step Vgs = 0.2 V.

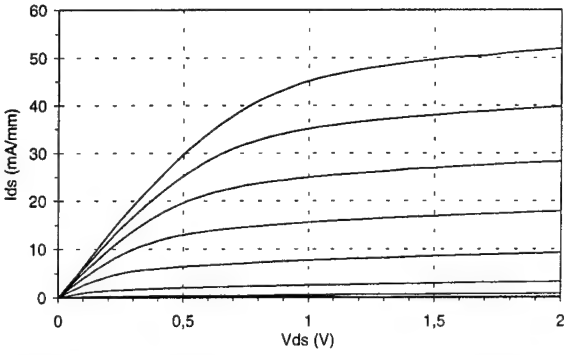

Fig. 4 : I-V measurement of 1µm-P-HIGFET. Vgs max = -1.6 V. Step Vgs = 0.2 V.

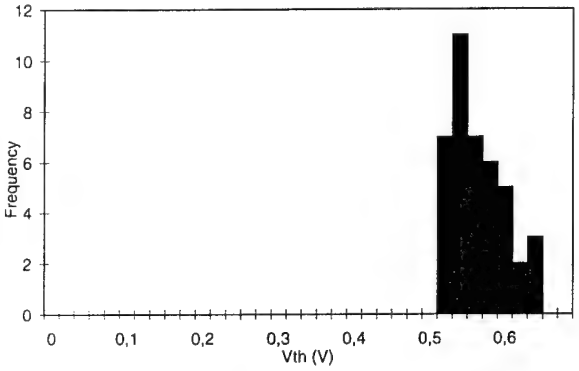

Fig. 5 : Threshold voltage distribution of 1µm-N-HIGFET. Standard deviation is 35 mV.

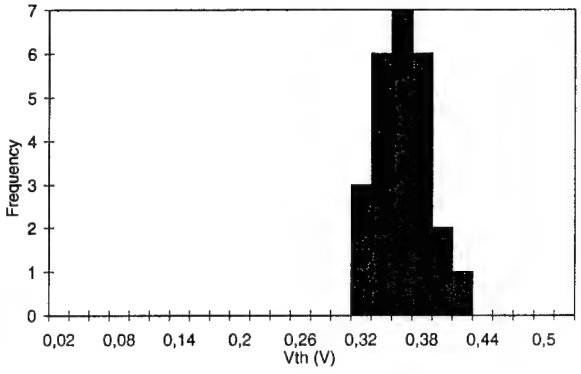

Fig. 6 : Threshold voltage distribution of 1µm-P-HIGFET. Standard deviation is 26 mV.

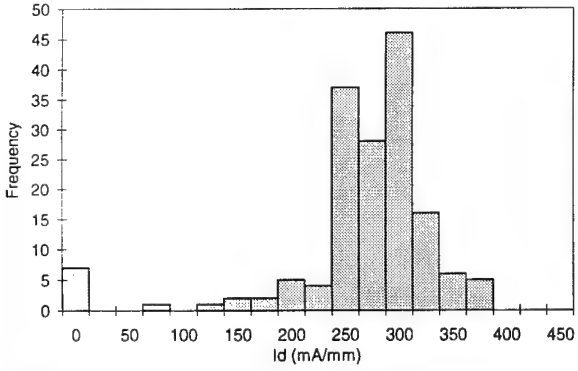

Fig. 7 : Ids distribution of 1µm-N-HIGFET at Vgs=2V.

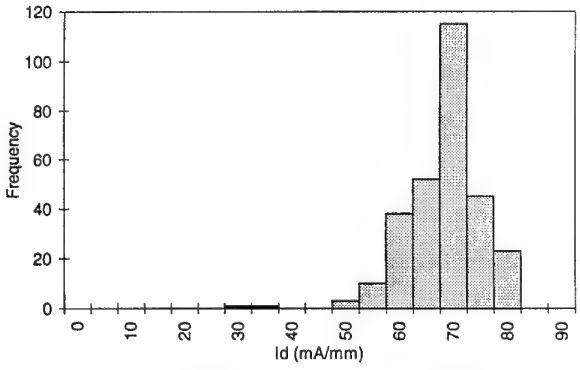

Fig. 8 : Ids distribution of 1µm-P-HIGFET at Vgs=-2V.

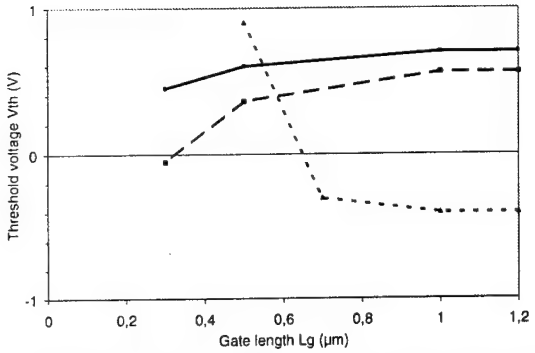

Fig. 9 : Analysis of short-channel effects on threshold voltage for N-HIGFET (dashed line), P-HIGFET (doted line) and N-HIGFET with sidewalls (solid line).

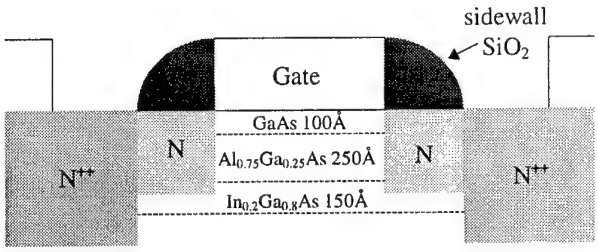

Fig. 10 : N-HIGFET structure with SiO_2 sidewalls

	N			P
Length (µm)	1	0.5	0.3	1
width (µm)	2*25	2*10	2*20	2*50
Ids (mA/mm)	340	420	530	79
Gm (mS/mm)	350	410	440	64
Gd (mS/mm)	9	11	29	3.7
Gm / Gd	39	39	15	17
Vton (V)	1.25	1.25	1.30	-2.3
S (mV/dec)	70	70	175	310
Ioff (A)	1.5n	1.4n	5µ	5.5µ
Ion / Ioff	2.3 e 6	4.2 e 6	3.2 e 3	1.4 e 3
K (mA/V^2mm)	430	560	370	45
Vth (V)	0.53	0.50	0.1	-0.36
Ft (GHz)	20	38	/	5
Fmax (GHz)	21	19	/	5

Table 1 : Typical parameter of pseudomorphic N and P-HIGFET (conventional process, without sidewalls)

	N		
Length (µm)	1	0.5	0.3
width (µm)	2*25	2*25	2*25
Ids (mA/mm)	310	420	510
Gm (mS/mm)	360	420	440
Gd (mS/mm)	22	32	45
Gm / Gd	16	13	10
Vton (V)	1.1	1	1
S (mV/dec)	83	88	100
Ioff (A)	30n	45n	90n
Ion / Ioff	5.1 e 5	4.7 e 5	2.8 e 5
K (mA/V^2mm)	400	450	400
Vth (V)	0.7	0.6	0.45
Ft (GHz)	17	35	44
Fmax (GHz)	20	28	31

Table 2 : Typical parameter of pseudomorphic N-HIGFET with sidewalls

Optical effects in p-channel InGaP/GaAs/InGaAs double heterojunction pseudomorphic MODFET

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A great deal of interest has been created in the study of optical effects in microwave devices due to their potentiality in optoelectronic integrated circuits for modulation and detection of high frequency optical signals in the optical communications systems.The optical responses of n-channel modulation-doped-field-effect-transistors(MODFETs) have been reported [1]. However, the studies on p-channel MODFETs, which is necessary for a high speed, low power consumption, complementary logic circuit with an n-channel MODFET, are rarely found. The main concern in p-channel MODFETs is to compensate and/or overcome the low hole mobility and the low valence band offset. Recently, for the first time, we have fabricated a p-channel InGaP/GaAs/InGaAs symmetric double heterojunction pseudomorphic MODFET, employing a strained $In_{0.13}Ga_{0.87}As$ layer as the channel layer and a high bandgap(1.89 eV) $In_{0.49}Ga_{0.51}P$ layer as the barrier layer to achieve better carrier confinement and improved carrier transport of two-dimensional hole gas in the channel.(Fig.1) The epitaxial layers were grown by a gas source MBE, and the fabricated transistor has a π-shaped gate structure with a gate length of 1 μm, a gate width of 240 μm, and both of the gate-source and the gate-drain spacing of 1.5 μm. Details of the material growth and the fabrication processes can be found in the recent publications[2,3], along with some characterization results.

In this presentation, we will summarize the main features of the optical effects on DC and microwave performances of the p-channel MODFET. A typical drain current-voltage characteristics is shown in Fig. 2, with and without optical illumination. The photocurrent, was usually larger for smaller gate-source voltages. In saturation regime, however, the photocurrent becomes independent of the gate-source voltage. The threshold voltage increased nonlinearly as we increased the incident optical power.(Fig. 3) The ratio of the saturated drain currents with and without the illumination, has a maximum at a certain gate-source voltage.(Fig.4) High (photo)responsivity has been obtained, especially at lower incident optical powers, and compared with a standard p-i-n photodiode[4].(Fig. 4) Optical effects on the microwave performances of the transistor are shown in Fig. 6, as increases in the current gain cut-off frequency (f_T) and the maximum available gain cut-off frequency (f_{max}), by 20 % and 10 %, respectively.

In addition, different models will be compared to understand the physical mechanisms involved in the optical effects on the DC and microwave characteristics of the p-channel MODFET.

References

[1] M. Arafa et al. *IEEE Electron Device Lett.*, 1996, **17**, (3), pp. 124-126
[2] H. J. Kim et al. *Electron. Lett.*, 1998, **34**, (1), pp. 126-128
[3] H. J. Kim et al. *Appl. Phys. Lett.*, 1998, **72**, (5), pp. 584-586
[4] P. R. Herczfeld, European Microw. Conf. Workshop Proc., 1994, pp. 3-8

P^+ - GaAs ($3X10^{19}cm^{-3}$: Be) cap layer	300 Å
Undoped $In_{0.49}Ga_{0.51}P$ Schottky layer	500 Å
P -$In_{0.49}Ga_{0.51}P$ ($2X10^{18}cm^{-3}$: Be) acceptor layer	100 Å
Undoped $In_{0.49}Ga_{0.51}P$ spacer layer	50 Å
Undoped GaAs	50 Å
Undoped $In_{0.13}Ga_{0.87}As$ 2-DHG channel layer	100 Å
Undoped GaAs	50 Å
Undoped $In_{0.49}Ga_{0.51}P$ spacer layer	50 Å
P -$In_{0.49}Ga_{0.51}P$ ($2X10^{18}cm^{-3}$: Be) acceptor layer	100 Å
Undoped GaAs buffer layer	2000 Å
Semi-Insulating GaAs Substrate	

Fig. 1 Wafer structure for the p-MODFET

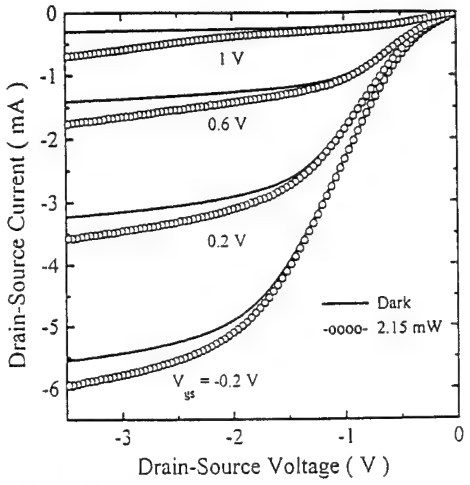

Fig. 2 Optical effects in *I-V* curves

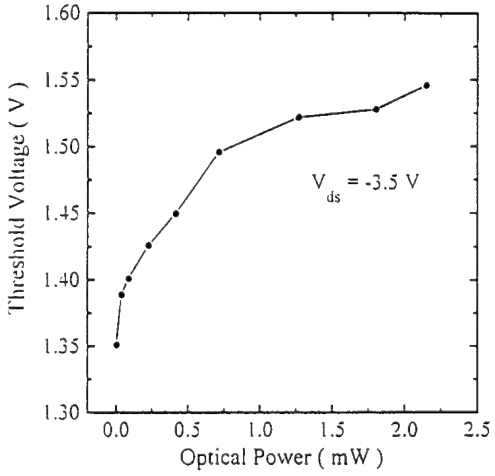

Fig. 3 Threshold voltage vs. optical power

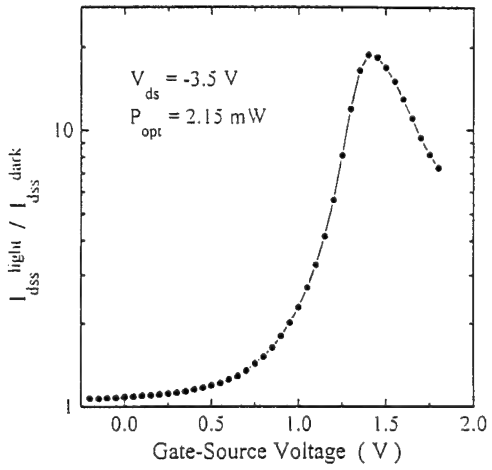

Fig. 4 Ratio of saturated drain currents vs. V_{gs}

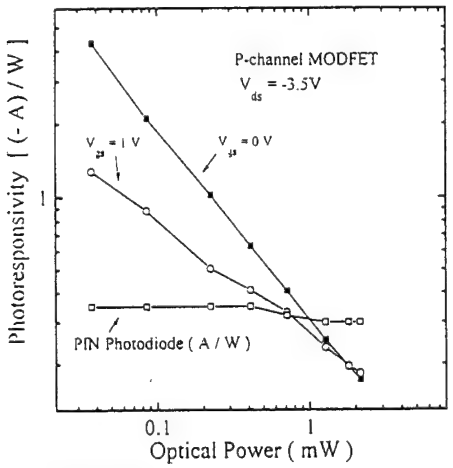

Fig. 5 Responsivity vs. optical power

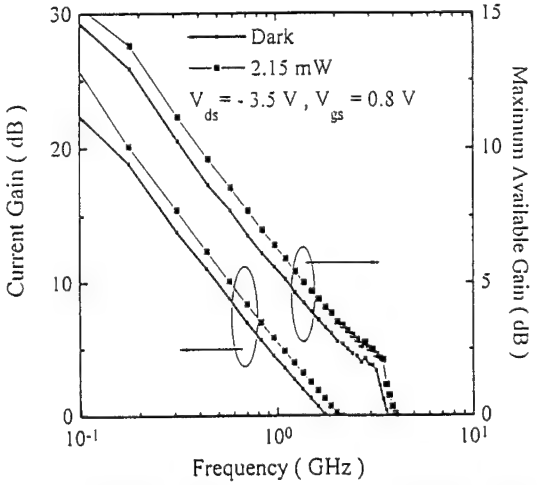

Fig. 6 Optical effects on microwave characteristics

First low temperature grown InP-channel HFET on GaAs substrate

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One proposed concept of monolithic integration of optoelectronic and electronic components without any degradation of the optimized optoelectronic device-properties is the growth of HFETs at very low temperatures (LTG). The P_{In} anti-side defect with first excited state located $120\,meV$ above the conduction band edge [1] leads to auto-doped n-type layers and makes LTG-InP a promising candidate for active layers. First devices fully grown on InP substrates at $300°C$ and below where external doping can normally not be activated electrically in III/V- materials were presented earlier [2]. For further development of the concept it will be essential to tranfer the low-temperature grown HFET-layers on other substrates than InP.

For the first time HFET structures grown on GaAs substrate at $300°C$ with LTG-InP channel will be presented in this investigation. The concentration of this P_{In} anti-site defects is connected with the growth temperature and V/III flux ratio. Therefore a strong influence of growth temperature on sheet carrier concentration and saturation current is found. Hall effect measurements revealed a sheet charge density of $1 \cdot 10^{13}\,cm^2$ and corresponding mobility of $1000\,cm^2/Vs$. LTG-AlInAs was used as gate contact layer [2]. The deoxidation of the semi-insulating GaAs substrates was performed at $625°C$ in the GSMBE chamber. The thickness of the thin layers still remains below the critical thickness for relaxation and therefore the layers are highly strained and under compressive stress.

The fabricated device structure with a thin LT-InP active channel layer of high doping concentration, sandwiched in a LTG-AlInAs buffer layer and a gate contact layer is shown in Figure 1. Due to the high sheet charge density no saturation of current could be achieved. A new technological redesign has lead to the DC output characteristics of LTG-InP FETs shown in Figure 2. The gatewidth was $50\,\mu m$ and $l_g = 1.5\,\mu m$. The channel current reaches a maximum open channel current density of $2.8\,mA/mm$. Due to difficulties with the Schottky layer pinch off is only partially possible. As in the case of InP the Schottky layer characteristics seem most critical. In comparison to the first HFET structure on GaAs, optimized HFET device structure and DC output characteristics grown on InP substrate are shown in Figure 3 & 4 [3].

In conclusion, this proof of concept will be starting-point for further improvements in both DC output characteristics by optimizing the gate contact layer and also sheet charge density. Furthermore, the fundamental possibility of transfering the growth of LTG-InP channel HFETs to GaAs substrates was shown leading to promising expectations of growth on other non-InP substrates.

References

[1] W. Chen et al., *J. Appl. Phys.*, **76,** (1994), pp. 600-602.

[2] B. Henle et al., *IPRM 97*, Hyannis, Cape Cod, Ma, USA, 11-15 May 1997, proc. 165-168

[3] B. Henle et al., *accepted for IPRM 98*, Tsukuba, Japan, May 1998

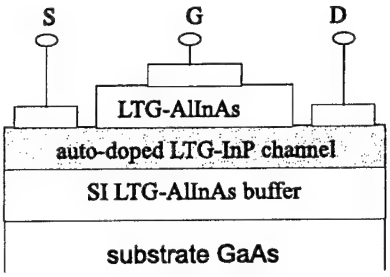

Figure 1: Schematic device structure of LTG-InP FET on GaAs substrate

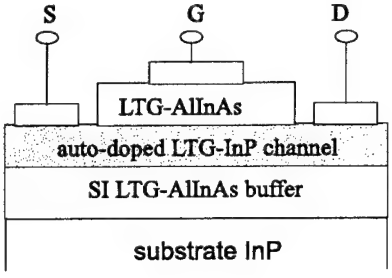

Figure 2: Schematic device structure of LTG-InP FET on InP substrate

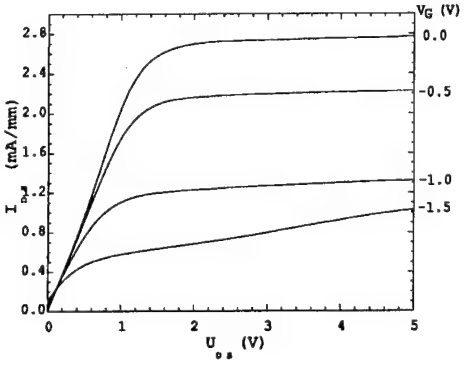

Figure 3: First output characteristics of LTG-InP FET grown on GaAs substrate at 300°C ($W_g = 50\,\mu m$ and $l_g = 1.5\,\mu m$

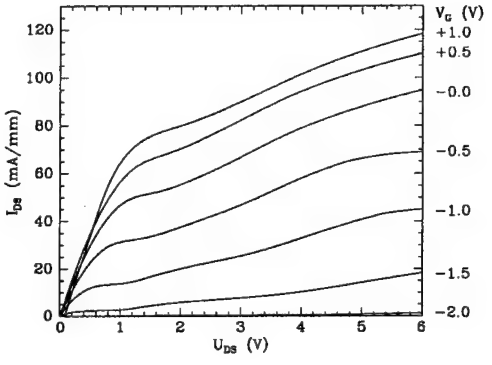

Figure 4: Output characteristics of optimized LTG-InP FET grown on InP substrate at 280°C ($W_g = 50\,\mu m$ and $l_g = 1.5\,\mu m$

Dual-Gate HEMTs with a closely spaced, floating second gate metalization:

A first approach by 2D-simulation

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An attempt is made to simulate the improvements in the characteristics of InAlAs/InGaAs HEMTs lattice matched to InP-substrate by adding a closely spaced second gate (fig.1, left), first by including overshoot but neglecting hot electron effects. This seems a valid approximation for $1/4\mu$m gate length technology comparing simulation with experiment [3], but certainly needs extension for downscaling gatelenght to sub-100nm. It is the first approach to adopt the commercial ATLAS [1] framework to such a device.

The results of the corresponding single gate structure are compared for variations in bias and geometry of the cascode arrangement. The floating second gate termination without DC or RF influence was chosen because of the feasibility of simulation and technological realisation (fig.1, right). Two dimensional drift diffusion with a $v_n = (\mu_0 E + v_{sat}\left(\frac{E}{E_0}\right)^\gamma)/(1+\left(\frac{E}{E_0}\right)^\gamma)$ $(\gamma = 4)$ velocity-field model fitted to Monte-Carlo results [1] serves as a worst case study due to the insufficient carrrier dynamics, which underestimate current, transconductance and other parameters. Nevertheless, the derived tendencies and proposed design rules are a starting point in the 8 dimensional parameter space.

In distinction to conventional dual-gate devices with two seperate FETs in series, here the spatial seperation of the gates is brought into the range of the drift region extention and the second gate is not contacted. The simulation results are well matched with a simple analytical expression using lumped elements for the drift length [2].

The advantage of this concept revealed by the decrease of C_{gd} and g_{ds} is based on the redistribution of the electric field. The potential is smoothed and the high field region enlarged for a closely spaced (d_{gg}=60nm) dual gate device (fig. 2b). In the example both gate regions are in saturation for V_{g1}=0V and the mean velocity averaged within the channel is well distributed (fig. 3). But already a change in V_{g1} of less than +/-0.2V (for a total gate bias swing from open channel to V_p of ΔV=2V) results in loss of symmetry and one gate region will fall back into the linear regime (fig. 2a and 2c). Thus this structure is quite critical to be designed and fabricated correctly.

However, the model shows that it is promising to alter the gate-drain drift region in HEMTs on InP. In the future hot carriers will be included by an energy balance model and alternative terminations for the second gate (e.g. RF grounded) will be investigated.

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[1] ATLAS is a trademark of SILVACO International

FIGURES

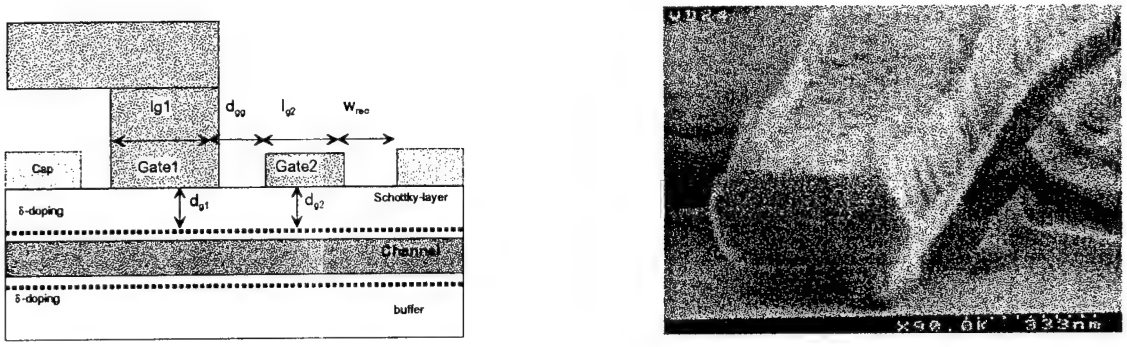

Fig. 1: Sketch of dual gate device and SEM picture of HEMT structure.

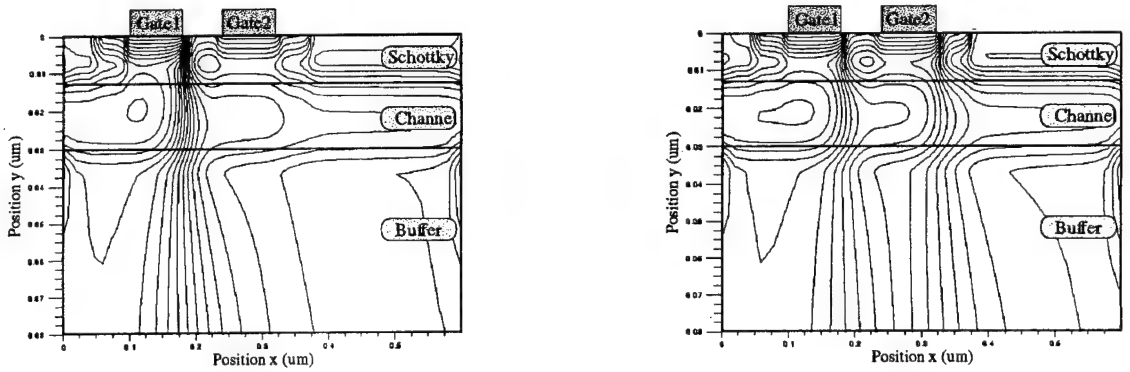

Fig. 2a and 2b: Potential distribution @V_{ds}=1V, V_{g1}=-0.2V, first gate in saturation(2a, left) and V_{g1}=0V ,both gates in saturation (2b, right).

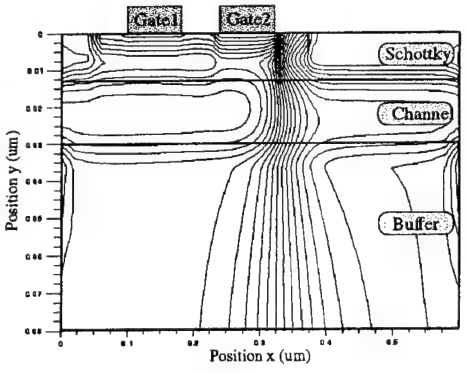

Fig. 2c: V_{ds}=1V, V_{g1}=0.2V, second gate in saturation.

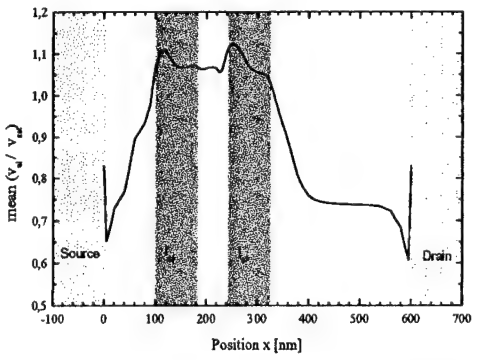

Fig 3: velocity distribution averaged over channel thickness, reflecting conditions of fig. 2b

[1] S.M Sze, "High Speed Semiconductor Devices", Wiley, New York, 1981

[2] S. Strähle, D. Geiger et al. "Drift Region Characteristics of InP-based HEMT Devices Evaluated by a simple Drift Region Model", Proc. IPRM 1994, pp 327, 1994

[3] L.Lee, W.Long, S.Strähle, B.Henle, H.Künzel et al., "Dual Gate HFET with Closely Spaced Electrodes on InP", Proc. IEEE Cornell Conf., 1995

A triple channel HEMT on InP (CAMEL HEMT) for large signal, high speed applications

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High speed, high breakdown voltage transistors are required in order to drive lasers and modulators. The InP-HEMT transistor is a good candidate for such applications, provided its channel material is well chosen. Transistors using GaInAs channels present high speed, whereas those using an InP channel have a low gate leakage current and a high breakdown voltage. To design a device with both of these advantages, a dual channel transistor (GaInAs/InP) has been already proposed [1, 2, 3], while a GaAs/AlGaAs double well channel has already been reported for high current [4].

In this work a triple channel HEMT structure grown on InP has been developed and named the "CAMEL HEMT". Starting from a dual channel (InGaAs/InP) HEMT that utilizes both the high electron mobility of InGaAs and the low impact ionization coefficient of InP, a third InGaAs channel as well as a quaternary carrier supply layer have been introduced to improve the electron transfer and thus the transistor performance. The structure of the new channel transistor is shown in figure 1.

As can be seen, the channel is made of four different layers :

(i) a first GaInAs channel 10 nm thick

(ii) a carrier supply layer made of a doping plane sandwiched between two undoped GaAlInAs layers which are used as spacers.

(iii) a second 10 nm thick GaInAs channel.

(iv) a n-doped InP sub-channel, 30 nm thick.

The AlGaInAs layer is used as a supply layer for electrons for the two GaInAs channels. The AlGaInAs supply layer and the GaInAs channels have been purposely chosen to be grown with the same group V element (As), in order to obtain better interfaces and higher electronic transfer from the doping plane to the GaInAs channel. With such a supply layer, electrons are more easily transferred to the InP under high electric fields. The two GaInAs channels insure conduction under low fields in the channel next to the source. At high fields almost all the electrons are transferred into the InP sub-channel.

The current gain cut-off frequency and the transconductance, vs Vgs characteristics of this transistor structure present a "Camel" like double bump due to the 2 GaInAs channels, that gave us the name "CAMEL HEMT" for this transistor structure.

Static and dynamic performances for a 0.8 µm gate length Camel HEMT are presented (figure 2 and 3 as well as tab 1). The results show that this new structure offers a very good trade-off between high breakdown voltage and current gain cut-off frequency.

[1] T. Enoki, K. Arai, A. Kohzen, Y. Ishii, « design and characteristics of InGaAs/InP composite-channel HFET's » IEEE Transactions on Electron Devices, Vol. 42, August 1995, pp.

[2] J. B, Shealy, M. Matloubian, T. Y. Liu, M. A. Thompson, M. M. Hashemi, S. P. Denbaars, U. K. Mishra, « High-performance submicrometer gatelength GaInAs/InP composite Channel HEMT's with Regrown Ohmic Contacts », IEEE Electron Device Letters, Vol. 17, November 1996, pp. 540

[3] H. Maher, J. Decobert, G. Post, A. Nezzari « Conception du transistor HFET à double canal GaInAs/InP » Journées Nationales Microondes, p. 172 , 1997

[4] G. W. Wang, Y. K. Chen, D. C. Radulescu, L. F. Eastman « A high-current Pseudomorphic AlGaAs/InGaAs double Quantum-Well MODFET » IEEE Electron Device Letters, Vol.9, NO. I, January 1988.

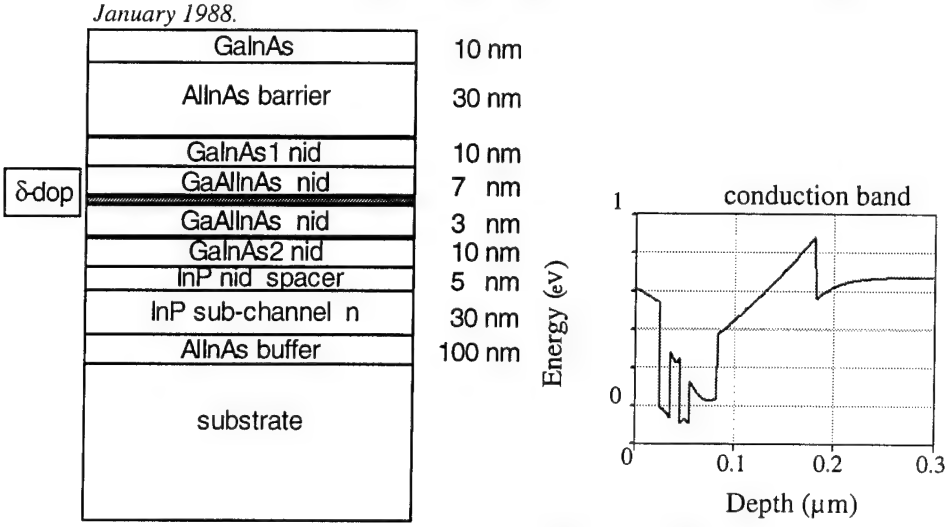

Fig 1 : Structure of the Camel HEMT and conduction band diagram

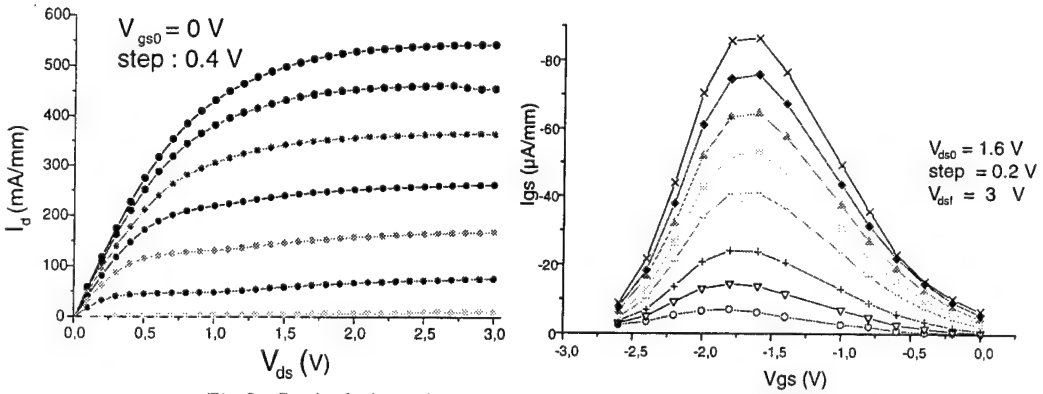

Fig 2 : Static drain and gate current characteristics of the Camel HEMT

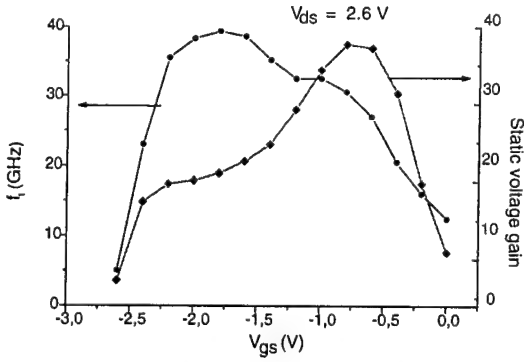

Fig 3 : Static voltage gain (g_m/g_d) of the transistor and current gain cut-off frequency, as a function of Vgs

Lg = 0.8 μm	I_{dss} (mA/mm)	I_g (μA/mm) at Vds =3 V)	g_{mmax} (mA/mm)	G_m/G_d max	Ft (GHz)	Fmax (GHz)	Breakdown voltage -on (V)
Camel HEMT	550	90	330	38	40	80	6.5

Table 1 : Performances of the Camel HEMT

Delta-doped GaAs MESFETs grown by low pressure MOCVD

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Delta-doping is very promising in applications for power field-effect transistors (FET). Among advantages of delta(δ)-doped FETs in comparison with standard MESFETs are high current density level due to channel carrier concentration easily being in the range 10^{12}-10^{13} cm^{-2}, high linearity, transconductance (because of small distance between the electron channel and the gate) and breakdown voltage. Nevertheless, it is difficult to achieve improved characteristics in real structures, since with decreasing the gate-channel distance (for δ-doped FET of the order of 30-50 nm) the local relief after gate recess should be less than 3-5 nm, moreover, etching homogeneity for the whole substrate should also be very high.

In this work we compare three types of δ-doped FETs: standard δ-doped FET with single δ-doped layer; single δ-doped channel with undergate wide-bandgap AlGaAs layer (15 nm thickness) to increase breakdown voltages; and double δ-doped layers (interlayer distance 15 nm) instead of single δ-doped channel for transconductance improvement. The net delta-doped channel concentration was 5×10^{12} cm^{-2} for both single and double δ-doped FETs. Contact cap layer consisted of 10 δ-doped layers in order to improve contact resistance. Transistor structures had gate 2.2×50 μm^2 and source-drain distance of 10 μm.

The samples were grown on semi-insulating and n^+ (Te-doped, 2×10^{18} cm^{-3}) GaAs substrates by low-pressure (100 mbar) metalorganic chemical vapor deposition at 600°C and 650°C. Thrimethylgallium, 10% arsine in hydrogen and silane (1500 ppm) diluted in argon were used. High concentration of the silane doping source allowed a doping time of only 5 sec, which in combination with a growth rate of 210 Å/min resulted in a rather short period of time (7 min) the δ-doped layers were kept at growth temperature. This was done to minimize the thermal diffusion of Si atoms. The capacitance-voltage profile of a δ-doped layer with $n=5\times10^{12}$ cm^{-2} (after cap layer etching) showed the full width at half maximum (FWHM) of 5.5 nm, which corresponds to spreading of impurity atoms of 3.0 nm (growth temperature 650°C). SIMS profiling was carried out on a Cameca IMS4f using 3 keV I_2^+ primary ions. The FWHM for double δ-doped layers is 3.0-3.5 nm, which with taking into account the resolution of the SIMS

technique for I_2^+ ions of 1 nm results in width of impurity distribution of less than 2.0 nm (growth temperature 600°C).

Saturation current for all transistors was in the range 120-200 mA/mm and pinch-off voltage 1.5-2.0 V. For single and double δ-doped FETs satisfactory breakdown voltage of 8 V was achieved. Drastic increase of breakdown voltage up to 25 V was observed for transistor with undergate AlGaAs layer, which could be explained by increase of the barrier under the gate and reduction of tunneling and thermal-field components of the gate current, which became essential for gate-channel distance of 30-40 nm.

The FET with a single δ-doped layer revealed extrinsic transconductance 140 mS/mm, the FET with undergate AlGaAs layer - 120 mS/mm and that with double δ-doped layer - 200 mS/mm for the gate length 2.2 μm.

A detailed investigation of conductivity dependence of high quality double δ-doped structures as a function of distance between δ-doped layers (concentration 3×10^{12} cm^{-2} per layer) will be also presented. At optimized spacer thickness of 190 Å, maximum in conductivity is observed both at 300 K and 77 K. The maximum exceeds the conductivity of the single δ-doped layer ($n=6\times10^{12}$ cm^{-2}) by 30 and 20 % at 300 K and 77 K, respectively.

40% improvement of transconductance for double δ-doped FET in comparison with single δ-doped FET is due to mobility and conductivity increase, which results from transition of a part of electrons from delta-doped planes to undoped spacer between them. This results in spatial separation of carriers and ionized impurities and reduction of scattering. The transconductance improvement is achieved via spatial rearrangement of doping atoms in two layers without increase of the doping concentration.

Thus, the usage of double δ-doping and undergate wide-bandgap material are very promising for power microwave transistors. Parameters of transistors could be further improved by optimizing concentration of δ-doped layers and distance between them, by changing the thickness and quality of undergate wide-bandgap material.

Session 6: Monolithic Microwave Integrated Systems (MMICs)

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W.H. Haydl, A. Tessmann, S. Kudszus, L. Verweyen, M. Neumann, A. Hülsmann, F. Steinhagen, A. Bangert, J. Rüdiger, M. Schlechtweg
Fraunhofer-Institut for Applied Solid State Physics, Freiburg — Germany

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A. Nagayama, M. Nishibe, T. Inaoka, N. Mineshima
Japan Radio Co., Saitama — Japan

17: 20 **Nonlinear Circuit Design for 77 GHz Automotive Applications**
L. Verweyen, H. J. Siweris, N. Neumann, U. Schaper, W. Haydl, W. Kellner, M. Schlechtweg
Fraunhofer-Institut for Applied Solid State Physics, Freiburg — Germany

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W. Schlaak, G. G. Mekonnen, W. Passenberg, R. Steingrüber, A. Seeger, Th. Engel, A. Umbach, H.-G. Bach
Heinrich-Hertz-Institut für Nachrichtentechnik, Berlin GmbH — Germany

17: 50 **Design and Modeling of Narrow Band InP-Photoreceiver OEICs Based on HEMTs and MSM Photodetector**
Th. Engel, G. G. Mekonnen, A. Umbach, V. Breuer, H.-G. Bach, E. H. Böttcher, D. Bimberg
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W-Band Coplanar MMICs using Cascode PM-HEMT Technology

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Abstract:

A number of W-band high performance and highly integrated MMICs in coplanar technology have been developed for radar and imaging applications. They are (a) 40-50 dB high-gain LNAs, (b) variable gain LNAs with a 70 dB gain control range, (c) wide band LNAs, (d) heterodyne receivers, and (e) FMCW radar sensors. The MMICs differ from the present state of the art through small size (3-8 mm^2), coplanar technology, and the extensive use of CASCODE amplifier techniques. A power gain density of more than 10 dB/mm^2 is obtained for high-gain amplifiers.

Coplanar W-Band MMICs :

A 0.15 µm gate length AlGaAs/InGaAs/GaAs PM-HEMT device technology, together with our coplanar circuit technology [1] has led to the development of a number of high-integration millimeter wave MMICs. Functional coplanar circuits of high complexity have been developed and are demonstrated here.

The MMICs described below make extensive use of modified cascode amplifiers, which are a further development of those described in the past [2]. They are characterized by an improved stability. These CASCODE circuits still offer significant advantages in gain versus chip area, compared to a conventional two-stage common source amplifier.

(a) High-gain LNAs:

High-gain amplifiers are desirable components for mm-wave imaging radiometers operating in the direct detection mode [3]. For such applications, low-noise amplifiers with 40-50 dB gain are required. Coplanar CASCODE four-stage amplifier MMIC measuring 1x3 mm^2 have been developed, having 40 dB gain, as shown in Fig. 1. The use and characterization of such high-gain MMICs is very critical because of the existence of parasitic plate- and surface-modes excited by the coplanar lines and discontinuities, causing the amplifier to become unstable. Special packaging techniques to suppress these undesired modes have been developed for this class of high gain amplifiers [4] .

(b) Variable-gain LNAs:

A gain control range of over 70 dB has been achieved with a four-stage CASCODE amplifier at 94 GHz. This is the highest gain control reported for a W-Band MMIC.

(c) Broad-Band LNAs:

Combining three CASCODE amplifier stages, a wide band amplifier MMIC measuring only 1x3 mm^2 was developed, having a bandwidth from 82 to 105 GHz with a gain of 18 dB.

(d) Heterodyne receivers:

Radar and imaging radiometer applications make extensive use of sensitive heterodyne receivers. Because of the presence of a mixer, LNAs with 20-30 dB gain are sufficient. We have developed single- and dual channel MMICs at 94 GHz, which incorporate balanced Schottky diode or single-ended resistive HEMT mixers. Two-stage CASCODE LNAs with a 6 dB noise figure are used in the antenna path, and single-stage CASCODE LNAs with up to 10 dBm output power are used in the LO path. The receiver MMICs have a typical conversion gain of 12 dB. A dual channel W- band wave guide module is shown in Fig. 2.

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(d) FMCW transmitter/receivers:

A compact coplanar 94 GHz FMCW MMIC was developed for radar and industrial sensor applications. The MMIC, shown in Fig. 3(a), measures 2x4 mm^2 and contains three MPAs, a VCO, a coupler, a balanced rat race diode mixer, and a two-stage LNA. The power output is 7 dBm at 94 GHz. The noise figure and the conversion gain of the heterodyne receiver are 6-7 and 9 dB, respectively. The VCO is electrically tunable over several GHz. The downconverted IF return signal from a 1 cm^2 metal target at a distance of 1.95 m from the antenna is illustrated in Fig. 3(b). Compared with a current state of the art FMCW transceiver MMIC [5], we have achieved a reduction in chip area by a factor of 3.

References:

[1] W. H. Haydl, A. Tessmann, K. Züfle, H. Massler, T. Krems, L. Verweyen, J. Schneider, "Models of coplanar lines and elements over the frequency range 0-120 GHz", 26th European Microwave Conference Proceedings, pp. 996-1000, Sept. 1996.

[2] M. Schlechtweg, W. H. Haydl, A. Bangert, J. Braunstein, P. J. Tasker, L. Verweyen, H. Massler, W. Bronner, A. Hülsmann, K. Köhler, "Coplanar Millimeter-wave IC's for W-band applications using 0.15 µm pseudomorphic MODFET's ", IEEE Journal of Solid-State Circuits, pp. 1426-1434, Oct. 1996.

[3] S. Weinreb, "Monolithic integrated circuit imaging radiometers", 1991 IEEE MTT-S International Microwave Symposium Digest, pp. 405-408, June 1991.

[4] T. Krems, A. Tessmann, W. H. Haydl, C. Schmelz, P. Heide, "Avoiding cross talk and feed back effects in packaging coplanar millimeter-wave circuits", IEEE MTT-S Digest, June 1998.

[5] K. W. Chang, G. S. Dow, H. Wang, T. H. Chen, K. Tan, B. Allen, J. Berenz, "A W-band Single-chip Transceiver for FMCW Radar," IEEE 1993 Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp. 41-44, 1993.

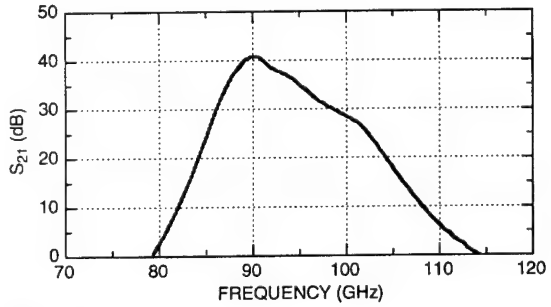


Fig. 1:
Power gain performance of a high gain coplanar 4-stage CASCODE LNA.

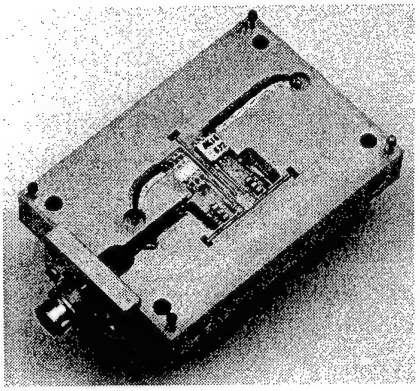
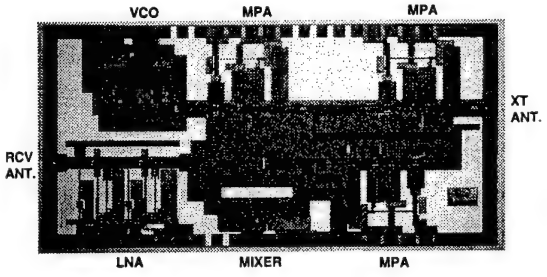
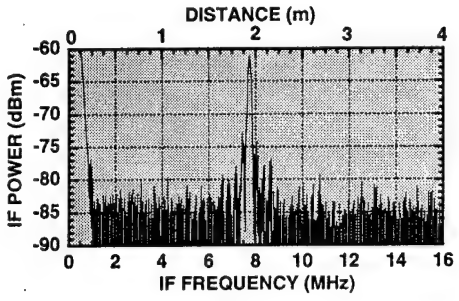


Fig. 2:
W-band wave guide module of 94 GHz dual channel heterodyne receiver.



(a)



(b)

Fig. 3:
(a) Coplanar 94 GHz FMCW radar sensor. The chip size is 2x4 mm^2.
(b) IF return signal for a detected object at a distance of 1.95 m.

Low Insertion Loss DP3T MMIC Switch for Dual Band Cellular Phones

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Abstract - A new type of dual-pole triple-throw(DP3T) double heterojunction monolithic microwave integrated circuit(MMIC) switch for use in digital cellular phones is proposed. The integrated circuit(IC) we developed exhibited a low gate leakage current of 400nA, and an insertion loss as low as 0.4dB even with added power of 34dBm at a frequency of up to 2.4GHz. $P1_{dB}$ was about 36dBm and a low distortion of 65dBc was also obtained.

1.Introduction

The continual drive to manufacture increasingly smaller portable electronic devices, such as cellular phones, has placed new demands on the power transmitter used in digital wireless communications.

Dual band cellular systems require a transmitter and receiver switch to connect one of these antennas to a transmitting power amplifier or one of two receiving circuits(an analog band and a digital band).

Therefore, a high-power DP3T switch with low insertion loss, high linearity, and low dissipation power is required for use in cellular phones.

Although development of many GaAs MMIC switches has been previously reported[1]-[3], those devices are SPDT or DPDT switches and cannot be operated above 36dBm. An alternative device technology capable of meeting these requirements is the heterojunction field effect transistor(HFET).

2. Design and Fabrication

The heterojunction structure we developed, illustrated in Figure 1, was grown by using Molecular Beam Epitaxy on semi-insulating GaAs substrates.

The epitaxial structure begins with a GaAs buffer layer. $Al_xGa_{1-x}As$ is formed on this buffer layer to act as a carrier barrier to inhibit channel width widening. The channel layer is formed using a narrow bandgap GaAs channel layer sandwiched between wider bandgap $Al_xGa_{1-x}As$ carrier confining layers. Above the layers comprising the device channel are a thin $Al_xGa_{1-x}As$ layer and a heavily doped N^+GaAs cap layer.

The low insertion loss of 0.4dB(including a circuit configuration loss of 0.1dB) can be achieved by decreasing the *on* resistance to 2.4-ohm. Assuming that the drain conductance is proportional to the gate width, the desired saturation current is calculated to be 220mA/mm. Isolation of 20dB requires 0.13pF of drain-source capacitance, and a low adjacent power density of 65dBc obtained with a 5dB back-off from P_{1dB} requires 2.5W/mm of power density with a drain bias of 3V.

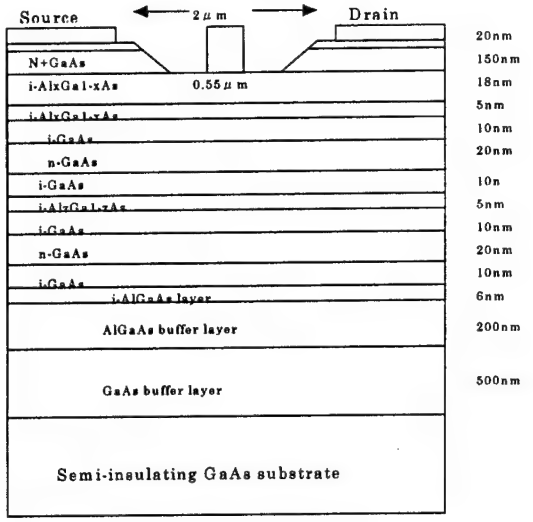

Fig.1 Cross-section of proposed device

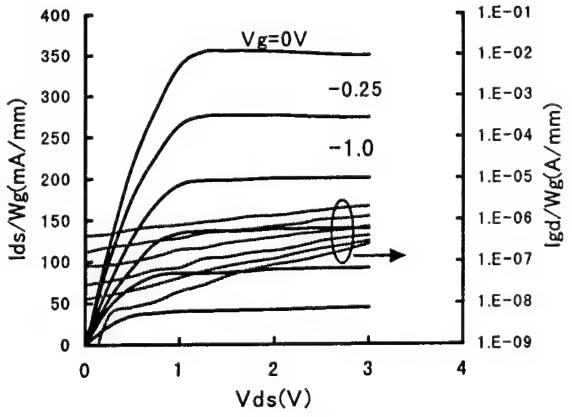

Fig.2 Current-voltage characteristics for the developed HFET

The mean Gm was 125mS/mm at Ids = 0.1 x Idss and the mean Idss was 250mA/mm at Vds = 3V. The measured results of the gate leakage current are shown in Figure 2.

A remarkably low leakage current was obtained using plasma-enhanced chemical vapor deposition of SiNx film in conjunction with an NH_4OH used to minimize the GaAs native oxide.

3. Circuit design

The DP3T IC switch we developed is shown in the Figure 3. This DP3T IC has two stacked FETs in order to obtain the high isolation required. For example, when the path between ANT1 and RX1 is the ON state, control signals S1 and S3 are in the OFF state, and signal S2 is in the ON state. Because of the high reflection of the RF leakage signal from the path between ANT1 and RX2 using SAW filters, high isolation can be expected. High isolation of the RX1 from the TX was obtained with only one stacked FET. This is because of the high impedance of the stacked FET achieved with the small stray capacitance of C_{GS}. The superior characteristics of the FET we developed make this configuration possible.

The widths of the FETs connected to ANT1 and the FETs connected to ANT2 were determined to be 2mm and 1mm, respectively.

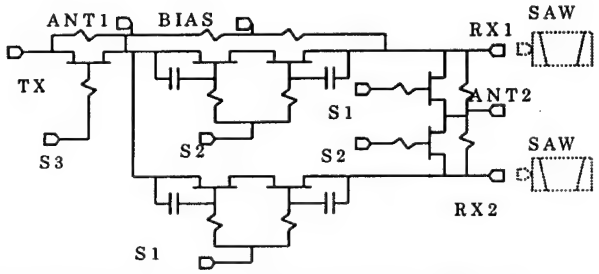

Fig.3 Schematic circuit of the developed IC

4. Performance

The RF power transfer characteristics are shown in Figure 4. An insertion loss of less than 0.45dB and an isolation of more than 60dB was obtained with an input power of 34dBm.

The insertion loss deteriorates in the ratio of approximately $3.3x10^{-3}$dB/dBm, but the isolation of mode than 60dB was obtained. This superior characteristic was achieved by employing low gate leakage current HFETs

The frequency response is also shown in Figure 5. The experimental results show that the developed IC can be used up to 2.4GHz.

The deterioration of insertion loss caused by reflection from mismatch can be neglected up to 2.4GHz.

The mean values of a 60dBc adjacent power level and a 65dBc third order harmonic power level with an added 33dBm RF power level, obtained by employing the present HFETs, show that the developed IC has excellent characteristics of low insertion loss and high linearity.

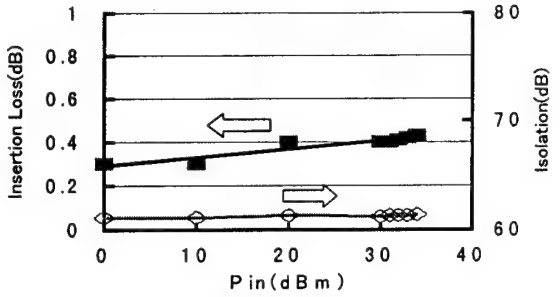

Fig.4 Power transfer characteristics of the developed IC at 1GHz

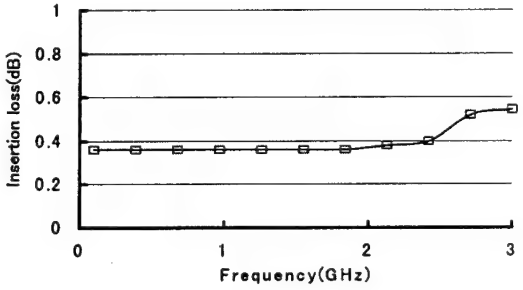

Fig.5 Frequency response of the developed IC

5. Conclusion

We developed an extremely low insertion loss MMIC switch by employing an improved HFET. This developed FET, having a mean value of 50nA/mm of gate leakage current with 33dBm of added RF power, demonstrated excellent linearity. These results show that the developed IC is well suited for use in portable digital telephone systems requiring high linearity.

References

[1] Kohama, K., T.Ohgihara., and Y.Murakami., "High power DPDT antenna switch MMIC for digital cellular systems" IEEE Journal of Solid-State Circuits, vol.31,No.10, (October 1996); 1406-1411.

[2] Ikeda, Y., et al., "A novel resonant-type GaAs SPDT switch IC with low distortion" Technical Reprt.of IEICE ED96-59,1996

[3] Tokumitsu, T., I.Toyoda., and Y.Ayasli., "A low- voltage, high-power T/R-switch MMIC using LC resonators" IEEE Trans.Microwave Theory Technol.,vol.43,no.5, (May,1995); 997-1003.

NONLINEAR CIRCUIT DESIGN FOR 77 GHZ AUTOMOTIVE APPLICATIONS

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I. INTRODUCTION

W-band radar systems for automotive applications have focused interest on cost effective integrated circuits on GaAs. With compact transmit and receive MMICs in coplanar technology, having a chip size of 3 x 2 mm² each, the required system performance at 77 GHz has been demonstrated [1, 2]. For meeting the targets of high volume markets, two goals are of crucial importance: Minimizing the total chip area necessary for a complete FMCW system at 77 GHz and reliable predictions of the nonlinear circuit performance. Both goals have been achieved in designing and fabricating a very compact integrated transceive MMIC with a 0.15 µm T-gate PMHEMT process in coplanar technology [3, 4]. An in-house analytical HEMT-model [5], implemented as symbolically defined device (SDD) in HP-MDS, has been used for performing harmonic balance simulations of the entire multifunction IC, comprising four transistors in the transmit path and up to three devices in the receive path. As will be shown in a more detailed description of the MMIC's electrical performance below, measured and simulated output power at 77 GHz as well as conversion characteristics agree very well, allowing a detailed in-situ power analysis of the transmit and the receive path.

II. MIXER TYPES

Various types of coplanar FET mixers have been investigated for use in the transceive MMIC [6, 7]. Resistive mixers, where the FET operates in a passive mode, achieved lower conversion loss than HEMT diode mixers. As can be seen in Fig. 1, the single ended and the balanced resistive mixer exhibit minimum conversion losses of 8 dB and 10 dB, respectively, for an LO power of only 3 dBm, when biased near pinch-off. The intermodulation characteristics of the resistive mixers, depicted in Fig. 2 have been

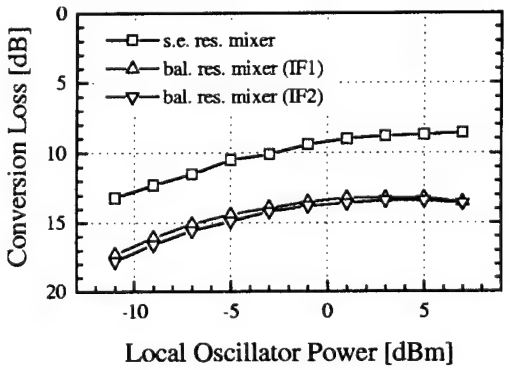

Fig. 1: Measured conversion loss of resistive MMIC mixers vs. LO power.

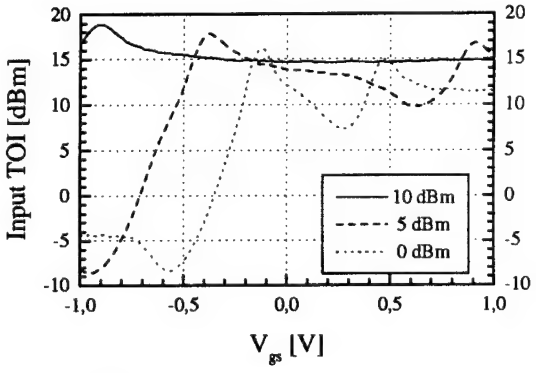

Fig. 2: Measured input third order intercept point of single ended resistive FET mixer vs. bias for different LO power levels.

investigated as a function of gate bias. For 5 dBm LO power and for a bias of 0.0 V, where the mixer needs minimum LO power for minimum conversion loss, an input TOI of +14 dBm was determined. By means of hot-cold-measurements, the DSB noise figure was determined. For an LO power of 3 dBm, DSB noise figures of 3 dB and 5 dB were measured for the single ended and the balanced version, respectively, for an IF of 1.5 GHz, being outside the 1/f-noise region of the HEMT.

III. TRANSCEIVE MMIC

In the transceive MMIC shown in the photograph of Fig. 3, the power of a 4-stage medium power amplifier is split in half via a rat-race coupler to the antenna port (P_4) and to the LO port of the mixer (P_2). The received signal is fed to a resistive FET mixer either directly or via a 2-stage low noise amplifier. The chip is suited for systems with separate TX and RX antennas. By minor changes in the air bridge layer, however, the receiver input can be connected to port 3 of the rat-race coupler. This modification enables the bidirectional operation of a single TX-RX antenna at port 4.

The measured and simulated performance of the transceive MMIC can be seen for both the transmit and the receive path in Fig. 4. An output power at the antenna port of 8.5 dBm was measured for an input power of only 0 dBm. A 2-stage amplifier compensates for the conversion loss of the resistive mixer of 8 dB and increases the overall conversion gain to 0 dB. The nonlinear performance of the transceive MMIC has been analyzed by harmonic balance simulations, using our in-house analytical HEMT model. For an input power of 0 dBm, the simulated output power of the 4-stage amplifier is 12.5 dBm at port 1, saturating at more than 15 dBm. At the LO port of the mixer (P_2) and at the antenna port (P_4), a power of 8 dBm is available. The dissipated DC power of the MMIC was 550 mW.

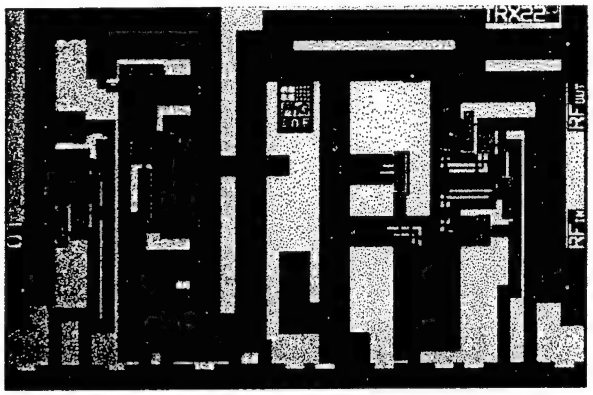

Fig. 3: Chip photograph of coplanar transceive MMIC (3x2 mm²).

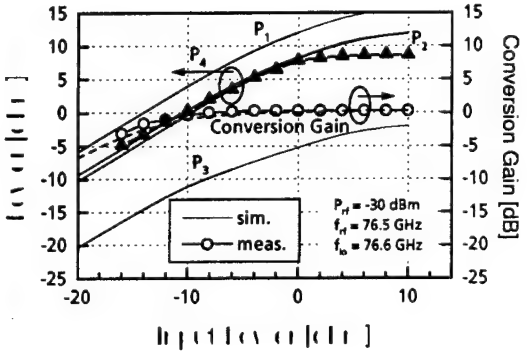

Fig. 4: Measured and simulated performance of transceive MMIC vs. input power.

[1] L. Verweyen, et al., "Compact Integrated Coplanar T/R-Modules for Automotive Applications," *IEEE MTT-S IMS Dig.*, Denver, pp. 243-246, 1997.

[2] J.-E. Müller, et al., "A GaAs HEMT MMIC Chip Set for Automotive Radar Systems Fabricated by Optical Stepper Lithography," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 1342-1349, 1997.

[3] H. J. Siweris, et al., "Low Cost GaAs PHEMT MMICs for Millimeter-Wave Sensor Applications," to be published at *IEEE MTT-S IMS*, Baltimore, 1998.

[4] L. Verweyen, et al., "Coplanar Transceive MMIC for 77 GHz Automotive Applications Based on a Nonlinear Design Approach," to be published at *IEEE MTT-S IMS*, Baltimore, 1998.

[5] R. Osorio, et al., "Large Signal Modeling and Verification for MODFETs Based on a New Analytical Gate Charge Equation," *4th Int. Workshop on INMWC Dig.*, Duisburg, pp. 95-100, 1996.

[6] L. Verweyen, et al., "Coplanar Integrated Mixers for 77 GHz Automotive Applications," *IEEE Microw. and Guided Wave Letters*, vol. 8, pp. 38-40, 1998.

[7] U. Schaper, et al., "70-90 GHz balanced resistive PHFET mixer MMIC," to be submitted to *Electronics Letters*, 1998.

A DC–21 GHz High-Gain Noise-Matched InP/InGaAs HBT Differential Amplifier

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Abstract

A high gain noise-matched differential amplifier has been successfully implemented. A gain of 21 dB, a 3 dB bandwidth of 21 GHz, and a noise figure $NF < 5$ dB has been achieved.

1 Technology and Model

For this design, a self aligned InP/InGaAs HBT with $f_T = 85\ GHz$ and $f_{max} = 130\ GHz$ [1] and its equivalent circuit model with associated noise sources were used. To validate the model a complete LF (Fig. 1(a)) and RF (Fig. 1(b)) small-signal and noise characterization as a function of emitter-geometry, temperature and bias-point were carried out [2].

2 Circuit Design

The amplifier uses a fully differential design to facilitate coupling to other circuits and setting of bias points. The schematic of the circuit is shown in figure 2. The three stage amplifier is divided into a noise matched input stage, a high gain and an output buffer stage. The noise-match is accomplished by using $1.5 \times 16\ \mu m^2$ HBTs (Q_{inl}, Q_{inr}) with an optimum source impedance around 50 Ω. The high gain stage consists of a Darlington amplifier with a parallel RC (R_E, C_E) as a series feedback to optimize the frequency response. The shunt feedback resistors R_{f1l} and R_{f1r} are designed for optimal gain-bandwidth performance. The feedback resistors R_{f2l} and R_{f2r} adjust the input impedance for minimum noise match.

3 Results

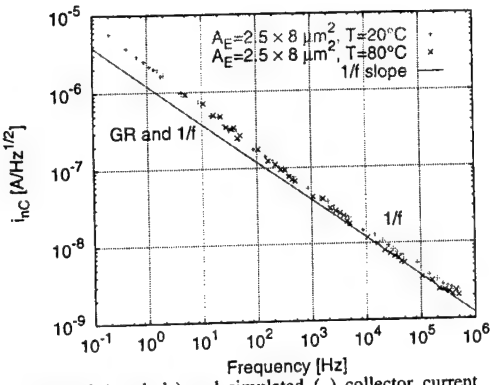
The gain and noise figure of the amplifier were measured on wafer in single-ended operation mode. The amplifier attains a gain of 15 dB, a 3 dB bandwidth of 21 GHz, and a noise figure of $NF < 8$ dB (Fig. 3(a)). Operating the amplifier in the differential mode adds an additional 6 dB to the gain and reduces the noise figure by 3 dB. Thus, a gain of 21 dB and a noise figure $NF < 5$ dB is expected to be achieved for differential mode operation. This presents a significant improvements over previously reported HBT wide-band amplifiers [3].

References

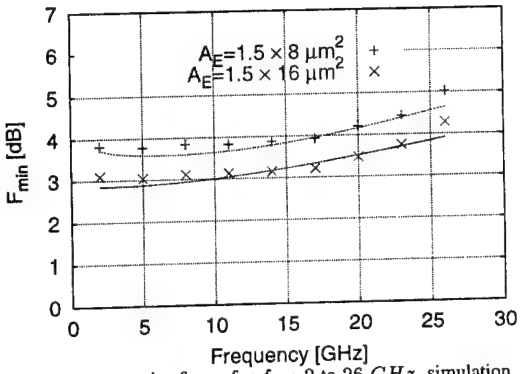
[1] R. Bauknecht, H. P. Schneibel, J. Schmid, and H. Melchior, "12 Gbit/s Laser Diode and Optical Modulator Drivers with InP/InGaAs Double HBTs," *Electronics Letters*, vol. 32, pp. 2156–2157, Nov. 1996.

[2] A. Huber, C. Bergamaschi, T. Morf, and H. Jäckel, "Broadband Noise Model for InP/InGaAs HBTs," in *Accepted for 10^{th} Intl. Conference on Indium Phosphide and Related Materials*, 1998.

[3] K. W. Kobayashi and A. K. Oki, "A DC-10 GHz High-Gain Low-Noise GaAs HBT Direct-Coupled Amplifier," *IEEE Microwave and Guided Wave Letters*, vol. 5, pp. 308–310, Sept. 1995.



(a) Measured (symbols) and simulated (–) collector current noise spectral density at the collector for $f = 0.2\ Hz$ to $500\ kHz$



(b) Minimum noise figure for $f = 2$ to $26\ GHz$, simulation (–), measurements (symbols)

Figure 1: Noise properties for different emitter areas and temperatures

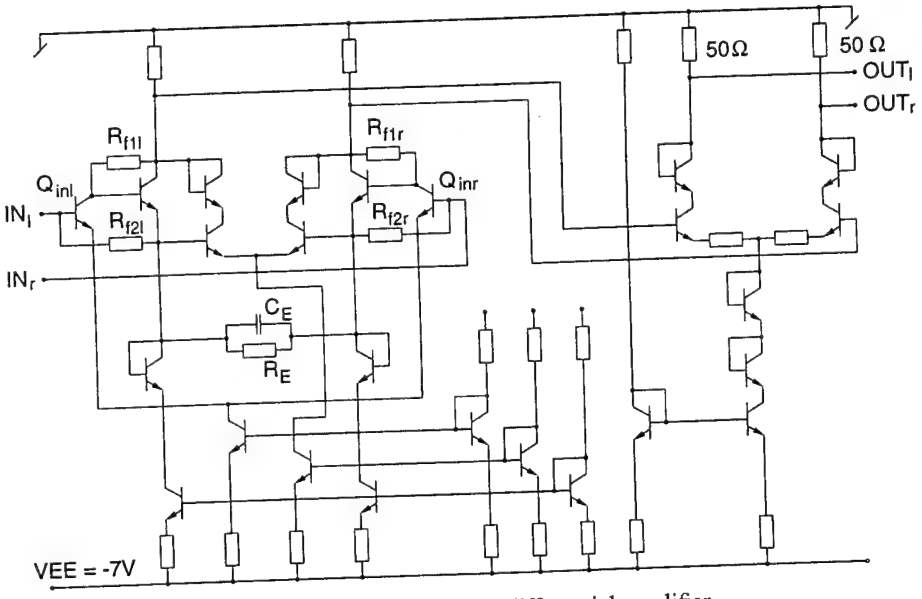
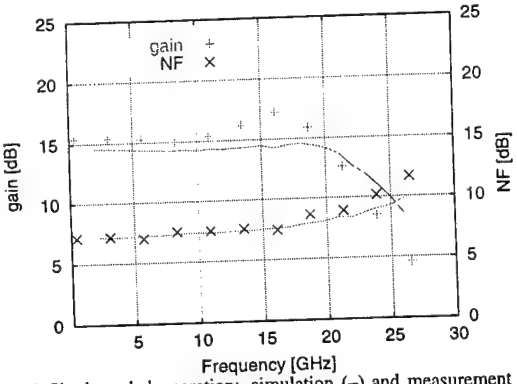
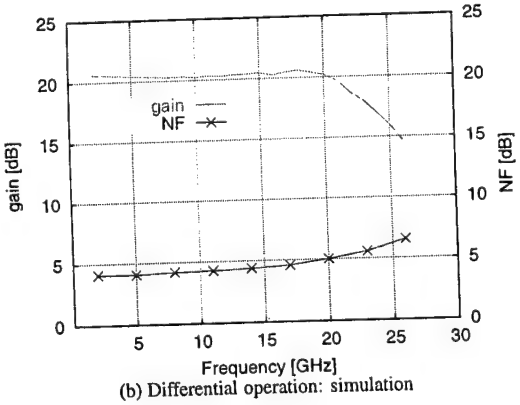


Figure 2: Schematic of the differential amplifier



(a) Single-ended operation: simulation (–) and measurement (symbols)



(b) Differential operation: simulation

Figure 3: Gain and noise figure of the differential amplifier

InP-HEMT Based Integration of Distributed Amplifiers for 40 Gbit/s Photoreceivers

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Optical front-ends play a major role in the bit rate upgrade of future telecommunication systems, world-wide prototype systems of which actually operate up to a bit rate of 40 Gbit/s /1/. Besides frond-ends also further electronic circuits like limiting amplifiers, decision circuits and clock recovery modules are needed for these high data rates. For cost effective fabrication within this product line, a common integration approach is highly desirable, which comprises the detector at the fibre end, the amplifiers as well as digital circuits for demultiplexing purposes. InP-based opto-electronics is a promising candidate for this goal /2/.

In this paper, we report on the InP-based monolithical integration of a distributed broadband amplifier aiming at a data rate of 40 Gbit/s, as part of a monolithical optical receiver OEIC for 1.55 µm wavelength. Our actual work is based on a validated circuit layout of a pinTWA integration as already published /3/, which uses HEMTs with optically defined gate structures. The high-frequency performance of this approach is limited to < 30 GHz due to gate lengths of about 0.6 µm obtained by optical gate lithography. For amplifiers well suited for 40 GHz bandwidth (40 Gbit/s data rates) and beyond HEMTs with transit frequencies in the range of 100/200 GHz for f_T and f_{max}, respectively, are needed. Therefore the HEMT gate lengths should be further reduced to ≤ 0.3 µm. Accordingly, we implemented an electron-beam writing process into the availabe HEMT / distributed amplifier process by using a high-resolution multilayer resist system. Fig. 1 shows the cut-off frequencies f_T and f_{max} of one of our e-beam gate HEMTs with 0.21 µm gate length vs. gate bias, where the maximum cut-off frequencies are achieved at zero gate bias as needed for distributed amplifiers schemes with simplified gate line biasing.

For reducing the development effort for an improved (f_{3dB} > 30 GHz) distributed amplifier and still having good process yield, we analyzed our circuit layout /3/ with respect to changes for 40 Gbit/s capability. Circuit simulations using the HEMT with e-beam written gate show (cf. Fig. 2), that the replacement of the "optical" HEMT by an e-beam gate HEMT and an accompanying change of the gate line termination resistance (25 → 29 Ω) will increase the bandwidth of the circuit considerably, while preserving good transfer characteristics of the transimpedance vs. frequency. Fig. 2a for reference shows the transfer characteristics of the transimpedance for the given layout /3/ using the HEMTs with optically defined gates (L_g = 0.6 µm). A bandwidth of 28 GHz is obtained, which has been confirmed experimentally /3/. By replacing the HEMTs in the circuit by e-beam gate HEMTs of L_g = 0.21 µm, see Fig. 2 b, the amplifier bandwidth is enhanced up to 40 GHz and beyond. Thus we expect that by simply implementing an e-beam gate process into our photoreceiver integration scheme will already yield 40 Gbit/s amplifiers, while still achieving good amplifier process yield due the simplicity of the circuit (only 4 HEMTs needed).

Consequently our e-beam gate HEMT process was adapted to our photoreceiver integration scheme of the distributed amplifier in coplanar line design. The process is based on a high-resolution multilayer resist system. This flexible process allows to generate mushroom-gates, Γ-gates or simple trapezoidal gates. In the actual amplifier we used a trapezoidal gate process due to the large process window and high yield; the gate resistance for this type of gate is uncritical for gate lengths down to 0.3 µm. The amplifier process is completely compatible to our 1.55 µm photoreceiver integration process, in which MOVPE growth of underlying semi-insulating GaInAsP:Fe optical waveguides is added. MIM capacitors and metal film resistors are used as passive devices, applied for the amplifier as well as for the biasing network of the photodiode. Finally coplanar waveguide interconnections employing air-bridges are formed by gold electroplating. A detailed view of our HEMTs with e-beam written gate structures coupled to coplanar transmission lines, is given in Fig. 3.

The distributed amplifier MMIC was characterized by on-wafer S-parameter measurements up to 50 GHz. Fig. 4 a shows the transimpedance as deduced from measured S-parameters vs. frequency. A bandwidth potential of 40 GHz is clearly visible. The unwanted ondulation of the transfer characteristics is due to the actual value of the gate line termination resistance in the range of 60 Ω in this first prototype amplifier. This is confirmed by simulation (cf. Fig. 4c), where the termination resistance was increased to this value. Nearly the same transmission properties are achieved for measured and simulated transimpedances. The gain difference to the reference curve b is due to the lower transconductance of 450 mS/mm of the HEMTs used in the integration (L_g = 0.4 µm) compared to the model HEMT with g_m = 680 mS/mm (0.21 µm gate length). With the adjustment of the gate termination to ≈ 29 Ω and the reduction of the gate length to 0.3 µm the predicted transimpedance characteristics (Fig. 4 b) will be achieved.
The high bandwidth of the amplifier makes it suitable for bit rates ≥ 40 Gbit/s. More recent results with improved gain and flatness will be shown at the workshop as well as progress on integration of the complete 40 Gbit/s photoreceiver.

This work was funded by the German BMBF and the Senate of Berlin within the framework of the PHOTONIK II programme.

/1/ E.Gottwald, A.Felder, H.-M.Rein, M.Möller, M.Wurzer, B.Stegmüller, M.Plihal, J.Bauer, F.Auracher, W.Zirwas, U.Gaubatz, A.Ebberg, K.Drögemüller, C.Weiske, G.Fischer, P.Krummrich, W.Bogner, and U.Fischer "Towards a 40 Gb/s Electrical Time Division Multiplexed Optical Transmission System" ICCT'96, Beijing, China, May 5-7, proceedings, pp. 60-63, 1996.

/2/ M.Yoneyama, A.Sano, T.Kataoka, A.Hirano, T.Otsuji, K.Sato, H.Miyazawa, and K.Hagimoto "40 Gbit/s optical repeater circuit using InAlAs/InGaAs HEMT digital IC modules" Electr. Lett. 33, pp. 1977-1978, 1997.

/3/ A.Umbach, S.van Waasen, U.Auer, H.-G.Bach, R.M.Bertenburg, V. Breuer, W.Ebert, G.Janssen, G.G.Mekonnen, W.Passenberg, W.Schlaak, C.Schramm, A. Seeger, F.-J.Tegude, and G.Unterbörsch "Monolithic pin-HEMT 1.55 µm photoreceiver on InP with 27 GHz Bandwidth" Electr. Lett. 32, pp. 2142-2143, 1996.

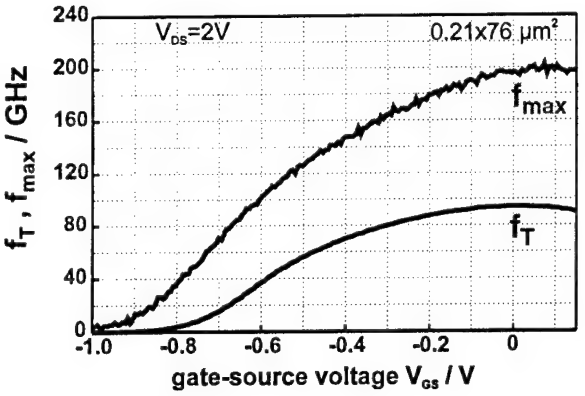

Fig.1: High-frequency behaviour (f_T and f_{max}(MAG)) of e-beam gate HEMT versus V_{GS}, measured at 25 GHz (gate length: 0.21 µm, gate width: 76 µm).

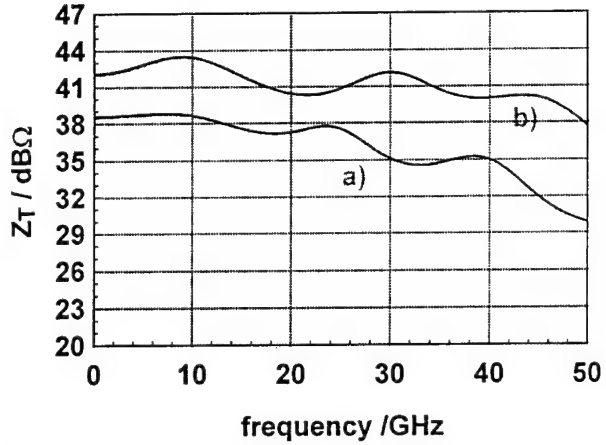

Fig.2: Simulated transimpedance vs. frequency of 4-stage distributed amplifiers:
a) with design according to ref. /3/ applying HEMTs with optical lithography gates (0.6 µm) and gate line termination of 25 Ω,
b) with enhanced bandwidth due to e-beam gate HEMTs (L_g: 0.21µm) and modified gate line termination resistance of 29 Ω.

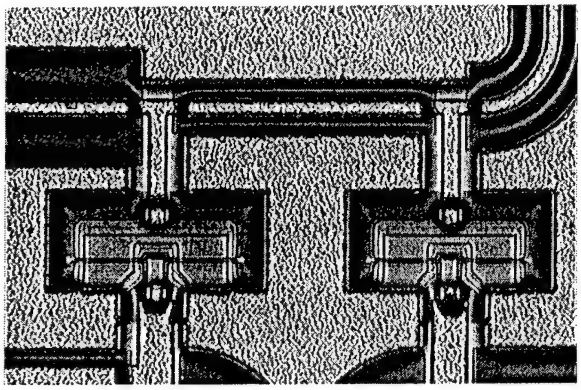

Fig.3: Microphotograph of a part of the distributed amplifier with four HEMTs with e-beam written gates. The total chip size is 1 x 3 mm².

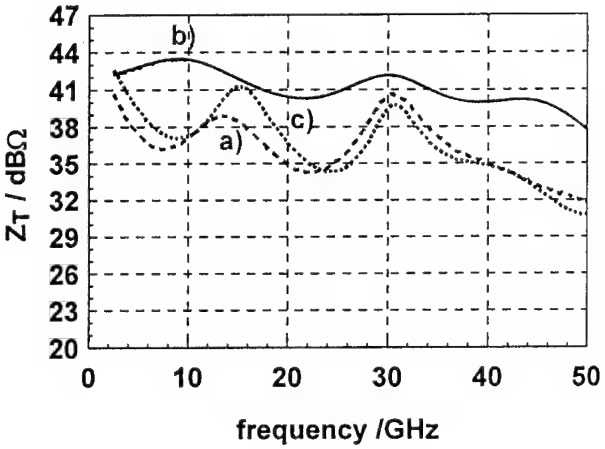

Fig.4: Transimpedance vs. frequency of distributed amplifier, obtained from S-parameters:
a) measured on fabricated TWA with e-beam gate HEMTs (L_g: 0.4 µm) and gate line termination of approx. 60 Ω,
b) design goal, for reference,
c) simulated behaviour according to real data adjusted to fabrication as in a).

Design and Modeling of Narrow Band InP-Photoreceiver OEICs based on HEMTs and MSM Photodetector

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Abstract: *The design and modeling of InP-based photoreceivers for narrow band applications in the K to V band range is presented. The OEICs consist of a top-illuminated submicron MSM photodetector and a three stage coplanar HEMT amplifier. Throughout the circuit design, chip layout and characterization a consistent strategy of device libraries is used, leading to a comfortable and reliable design process.*

Introduction

Optical receivers will play a major role in fiber-fed cellular mobile communication systems /1/. We report on the design and modeling of InP-based photoreceiver OEICs for λ=1.55 µm, which might be employed in such systems. The OEICs combine two types of high-speed devices, a submicron Metal-Semiconductor-Metal photodetector (MSM PD) based on InP:Fe/InGaAs:Fe, and quarter-micron High-Electron-Mobility-Transistors (HEMT) incorporating an InGaAs/InAlAs/InP layer stack. The circuit design of the OEIC has been done based on verified device models, which were implemented in the microwave design environment HP EEsof "libra". The successful fabrication and characterization of the OEICs will be published soon.

OEIC Design

The photodetector and the amplifier of which the OEIC is composed have been designed as separate building blocks working within a 50 Ω environment.

The photodetector building block consists of the MSM PD and a coplanar bias-T. The coplanar bias-T includes coplanar waveguides (CPW), a coplanar T-junction and metal-insulator-metal (MIM) capacitors, matching the MSM PD to an impedance of 50 Ω over the frequency range of interest.

The following three stage HEMT amplifier building block consists of CPWs exhibiting an impedance of 50 Ω, coplanar X-junctions, MIM capacitors, NiCr resistors and HEMTs. As shown in Fig. 1 each stage includes two coplanar networks reactively matching the HEMTs' impedances between the stages and at the inputs and outputs of the amplifier within a the narrow band. To obtain stability for the amplifier the stages NiCr resistors are employed. The ends of the CPW lines were shorted by coplanar integrated MIM capacitors coupled to the ground plane. The cascaded stages are coupled by inline MIM capacitors. During the design procedure the lengths of the coplanar waveguides were varied by an optimizer to meet a specified narrow band frequency response of the amplifier, and minimum signal reflection in the passband.

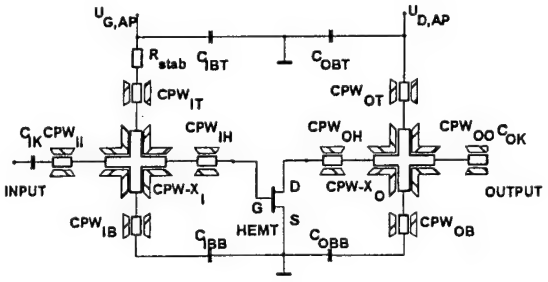

Fig. 1: Stage of the coplanar narrow band amplifier

Modeling of Components

For modeling the MSM PD an illumination sensitive large-signal noise model has been developed. It contains photo drift current, shot-noise sources /2/ controlled by the incident light power, and intrinsic RLC elements (see Fig. 2). The photo drift currents of electrons I_n and holes I_p are calculated as a product of incident light power P_{opt}, quantum efficiency η and a frequency response term $F_{n/p}$ derived from the Fourier transform of a triangular approximation to a MSM PD's impulse response.

$$\eta = (1 - R_{InP}) \cdot \frac{G}{G+B} \cdot \exp(-d_{InP} \cdot \alpha) \cdot (1 - \exp(-d_{InGaAs} \cdot \alpha_{InGaAs}))$$

$$I_{n/p} = \frac{1}{2} \cdot \frac{q}{h \cdot \nu} \cdot P_{opt} \cdot \eta$$

$$F_{n/p}(\omega) = 2 \cdot \left(\frac{1 - \exp(-j \cdot \omega \cdot \tau_{n/p}) - j \cdot \omega \cdot \tau_{n/p}}{(\tau_{n/p} \cdot \omega)^2} \right)$$

$$I(\omega)_{photo} = F_n(\omega) \cdot I_n + F_p(\omega) \cdot I_p$$

The drift time parameters $\tau_{n/p}$ are depending on the average carrier drift paths of electrons and holes and their saturated drift velocities. The leakage current and the resulting shot noise are modeled by two additional sources. The simulation results were verified by comparison with measurements /3/ of prototype MSM PDs.

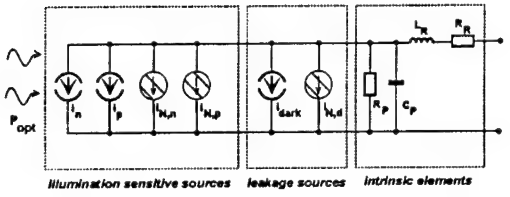

Fig. 2: Illumination sensitive MSM PD noise model

For the HEMTs a small-signal noise model and a large-signal model have been implemented, based on s-parameter measurements within the 0.05-50 GHz range and noise measurements within the 3-26 GHz range. The small-signal noise model consists of three areas /4/ and contains noise sources modeling gate-leakage noise, channel noise, 1/f noise and thermal noise of resistive elements (see Fig. 3). The U-shaped-gate HEMTs were designed to have a gate length of L_G=0.26 µm and a gate width of W=75 µm. The fabricated prototypes show an extrinsic transconductance of g_m=490 mS/mm and cut-off frequencies of 58 GHz and 120 GHz for f_T and f_{max}, in good agreement with simulations.

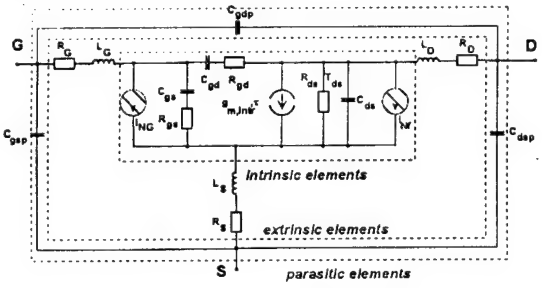

Fig. 3: Small-signal noise model of HEMT

For the coplanar waveguides the model provided by HP EEsof "libra" has been used with the geometric parameters established by the fabrication process.

The coplanar T- and X-junctions /5/ have been modeled with series inductors from each port connected to a node including a grounded capacitor. This lumped element approch is valid up to 140 GHz.

Modeling of OEIC

The simulations of the whole OEIC were performed in the frequency domain from 1 GHz to 80 GHz with an optical input power of P_{opt}=0 dBm.

As depicted in Fig. 4 the OEIC exhibits a responsivity of about 5.1 A/W resulting in an optical transimpedance of $Z_{T,opt}$=255 V/W within the narrow band around 37 GHz. The 3 dB bandwidth is 5 GHz.

Integration over the narrow band of the simulated output noise power densities of the MSM PD and the OEIC result in an output noise power of $P_{N,MSM}$=-67.5 dBm and $P_{N,OEIC}$=-34.1 dBm. With an amplifier narrow band gain of G=25 dB this results in an input noise level of $I_{N,MSM}$=26 pA/√Hz and $I_{N,OEIC,IN}$=70 pA/√Hz for the MSM PD and the OEIC, respectively. Thus the amplifier exhibits a noise figure of 8.5dB.

Conclusion

We presented the design and modeling of a monolithically integrated photoreceiver for the use in the 37 GHz range. According to the simulation the designed prototype OEIC exhibits a responsivity of about 5.1 A/W at a wavelength of 1.55 µm. The successful fabrication and characterization of such OEICs will be published elsewhere.

Since the circuit design, chip layout and characterization follow a consistent strategy of device libraries the presented procedure permits a comfortable and reliable design of OEICs at other narrow band frequencies using our approved integration concept.

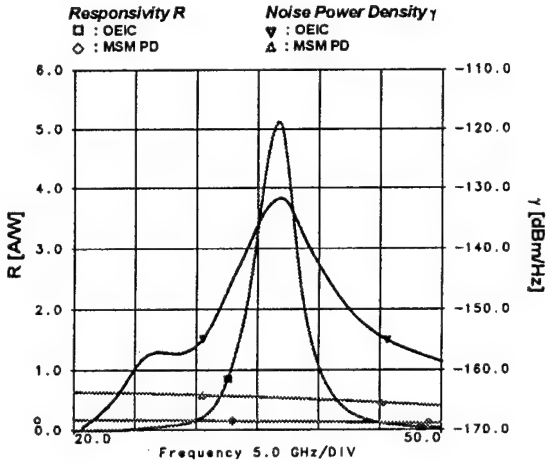

Fig. 4: Simulated frequency response of MSM PD and OEIC

Acknowledgement

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References

/1/ O. WADA:
"Advances in InP-Based Optoelectronic Devices and Circuits for Optical Communication, Interconnection and Signal Processing",
Proc. of the 9th Conf. on IPRM, May 1997

/2/ H. SCHUMACHER et. al.:
"Noise Behavior of InAlAs/GaInAs MSM Photodetectors",
IEE Electronics Letters, 26th April 1990, pp.612-613

/3/ E.-H. BÖTTCHER et. al.:
"Ultra-Wide-Band (>40 GHz) Submicron InGaAs Metal-Semiconductor-Metal Photodetectors",
IEEE Photonic Technology Letters,
Vol. 8, September 1996, pp.1226-1228

/4/ P. J. TASKER et. al.:
"New MODFET small Signal Circuit Model Required for Millimeter-Wave MMIC Design: Extraction and Validation to 120 GHz",
IEEE MTT-S Digest 1995, WE3C-1

/5/ K. BEILENHOFF et. al.:
"Analysis of T-Junctions for Coplanar MMICs",
IEEE MTT-S Digest 1994, pp.1301-1304

Session 7: Millimeter Wave and Terahertz Electronics

8: 00 **Circuit Considerations for Terahertz Electronics**
C. M. Mann — *invited*
Rutherford Appleton Laboratory, Chilton, Didcot, Oxfordshire — UK

8: 30 **New Doping-Barrier Varactor (DBV) for mm-Wave Multiplier Applications**
J. Freyer, M. Claassen
Technische Universität München — Germany

8: 40 **THz Characterization of High-speed Transmission Lines**
M. Nagel, H. M. Heiliger, T. Dekorsy, H. Kurz, R. Hey, K. Ploog
RWTH Aachen — Germany

8: 50 **Terahertz Range Electrical Generation of Current Oscillations in Nanostructures**
V. Mitin, A. Korshak, Z. Gribnikov
Wayne State University, Detroit — USA

CIRCUIT CONSIDERATIONS FOR TERAHERTZ ELECTRONICS

by C. M. Mann

Rutherford Appleton Laboratory (RAL), Chilton, Didcot, Oxfordshire, UK

ABSTRACT

In recent years there has been much interest in the use of terahertz radiometers for making measurements of the stratospheric hydroxyl radical (OH). This molecule plays a critical role in all cycles of ozone destruction and also acts as an oxidant for harmful gases in the atmosphere.

The main focus of recent work in both Europe and the USA has been on the demonstration of a 2.5THz radiometer front end that is capable of making such measurements from space.

Heterodyne detection is the preferred spectroscopic technique used to retrieve the data and this requires the use of a heterodyne mixer to perform the first frequency down conversion. The mixer works by combining the signal to be measured with a Local Oscillator signal in a non-linear device, the difference frequency typically Å 10GHz is then amplified and detected. This mixer actually has to operate as an electrical circuit at the signal frequency of 2.5THz. It must also exhibit the following characteristics. Firstly it must be reliable and operate at ambient temperatures whilst still providing state of the art sensitivity. In addition, as it is the first optical element in the front-end its radiation properties must be near perfect with side lobes less than 20dB.

The only semi-conductor device that is sufficiently fast at room temperature is the Schottky diode. However, whilst the intrinsic Schottky diode can easily operate at these frequencies, if the circuit in which it is embedded is poorly conceived then the diode may not be able detect any signal through no fault of its own. Therefore before comparisons can be made as to the suitability of a particular diode, accurate knowledge of the diode operating conditions is essential. Until recently only crude RF circuits such as corner reflector mixers could be implemented but in the past few years terahertz waveguide circuits have been demonstrated.

Recent successes at RAL in this area include the fabrication of a 2.5THz corrugated feedhorn and its use as the antenna for a state of the art 2.5THz Schottky diode waveguide mixer. This mixer makes use of a novel micromachined lithographic 'whisker' which has a number of advantages that will be discussed. This technology is rapidly reaching maturity and attention is now aimed towards the integration of waveguide cavity and terahertz RF circuitry. This can be achieved with

the use of a variety of micromachining techniques. Various routes will be examined and the relative merits of each will be discussed. A fabrication scheme that promises to fulfil both RF and integration requirements will be presented.

New Doping-Barrier Varactor (DBV) for mm-wave Multiplier Applications

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Technische Universität München

All-solid-state power sources are needed for a wide range of millimeter-wave and Terahertz applications. As with increasing frequency power generation from solid-state fundamental oscillators is limited, above about 200 GHz frequency multipliers are used. The Schottky varactor is the most commonly used multiplier device though several novel devices with symmetric capacitance-voltage characteristics like the hetero-barrier varactor show diverse advantages, e.g. for triplers no bias and idler circuits are necessary. This leads to simpler circuits and is important if monolithic power addition from several sources is aspired. The ratio of maximum to minimum capacitance C_{max}/C_{min} and the onset-voltage for current flow are measures for the quality of the varactor.

In this paper, a new doping-barrier varactor (DBV) with symmetric capacitance-voltage characteristic is proposed which can be applied for millimeter-wave multipliers. Theoretical as well as first experimental results are given.

The device consists of a highly doped $n^+p^+n^+$ layer sequence embedded into low doped n^--layers on both sides with n^+-zones for the contacts (see Fig. 1a). The width and doping of the p^+-layer and the two adjacent n^+-layers are designed such that the depletion layers of both p^+n^+-junctions merge to one zone which is free of mobile carriers. Under these conditions, the space charge of the ionised doping atoms in the $n^+p^+n^+$ structure leads to a bump in the conduction band as can be seen in Fig. 1b for the case of zero bias. This represents a potential barrier for the electrons. The same bump arises also in the valence band. It must be distinctly lower than the band gap so that the valence band remains sufficiently below the Fermi level to keep the concentration of the holes low.

If a bias voltage is applied (see Fig. 1c, negative voltage at the left contact) carrier accumulation occurs in front of the barrier in n^+-layer. This lowers the height of the potential barrier. On the opposite side of the barrier, a depletion layer is created which, due to the relatively low doping concentration of the n^--layer, extends widely into this layer. This leads to the desired modulation of the capacitance of the device. If the polarity of the bias is changed, a mirrored band shape with the same depletion layer width appears leading to a symmetric capacitance-voltage characteristic. Therefore, similar to the hetero-barrier varactor, the DBV is adapted for multiplier applications in the millimeter-wave fields.

With increasing voltage, the height of the barrier is reduced and the electrons can overcome the barrier by thermionic emission and/or diffusion. The onset of current limits the maximum rf-voltage amplitude. However, as compared to the hetero-barrier varactor, the barrier in the DBV can be essentially higher (for proper design up to 1 eV in GaAs) so that higher rf-voltage amplitudes may be applied with the advantage of higher input and output power of the varactor.

Simulations for GaAs DBV's show that the needed doping concentrations and widths of the inner n^+- and p^+-layers of the DBV are well within the potential of a typical MBE system. The best results for C_{max}/C_{min} are achieved if charge neutrality in the $n^+p^+n^+$ barrier layer is realised. Table 1 shows as an example doping concentration and thickness of the different layers of a DBV for tripler application from 100 GHz to 300 GHz. The doping concentration in the n^--layers is designed to $3\ 10^{17}$ cm^{-3} with a width of 200 nm to avoid velocity saturation. For this device the ratio of C_{max}/C_{min} is 4 and the maximum allowable voltage is about 10 V.

Fig. 2 shows the very first experimental results for the capacitance-voltage characteristic of a DBV structure after Table 1. C_{max}/C_{min} is only about 3 indicating that the varactor is not yet optimised from the technological point of view. Next work will be to fabricate more properly the device structure and to test the DBV for tripler application in the mm-wave region. Additionally, the implementation of larger band gap material (GaAlAs) for the inner p^+- and n^+-layers of the varactor is planned to further increase the barrier for electrons.

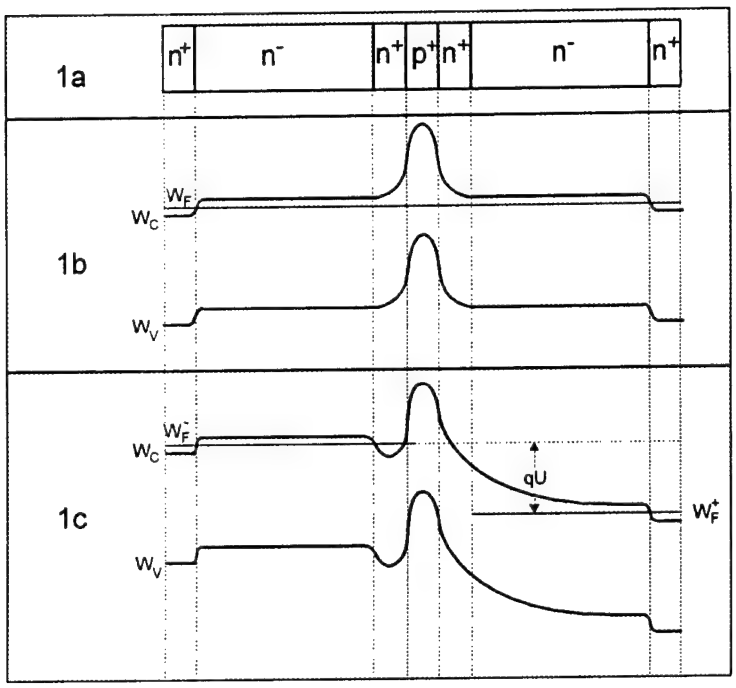

Fig. 1: Schematic representation of a DBV
1a) layers sequence, 1b) energy band structure for zero bias, 1c) energy band structure for applied bias voltage

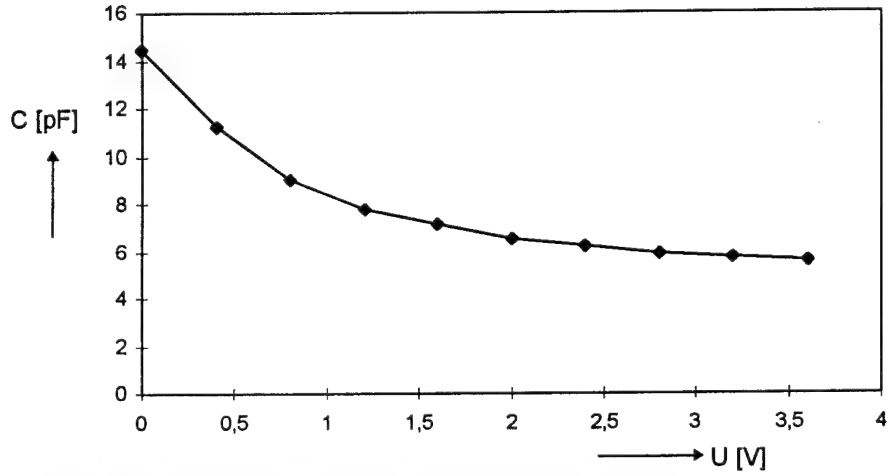

Fig. 2: Measured capacitance-voltage characteristic of DBV

layer	n+	n	n+	p+	n+	n	n+
doping [cm^{-3}]	$3\ 10^{18}$	$3\ 10^{17}$	$5\ 10^{18}$	$2\ 10^{19}$	$5\ 10^{18}$	$3\ 10^{17}$	$3\ 10^{18}$
thickness [nm]	50	200	20	10	20	200	50

Table 1: Doping concentration and layer thickness of DBV

THz Characterization of High-speed Transmission Lines

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Currently there is a strong interest in the design and fabrication of monolithic microwave integrated circuits (MMICs) accessible for the wide consumer market with low production costs. Very promising are the recent developments based on silicon. $Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors (HBTs) are now reaching cut-off frequencies beyond 110 GHz.[1] In order to exploit this potential special transmission lines matched to low-resistivity Si substrates are necessary. An optimal qualified type of waveguide for this application are thin-film microstrip (TFMS) lines with a low-permittivity polymer layer over a ground metalization with a signal conductor on top (see Fig. 1). The TFMS lines provide weak attenuation, exceptionally low dispersion, high signal speeds and high packaging densities independent of substrate characteristics. The production of these waveguides is compatible to standard Si technology.[2]

For investigations of electric signals in the mm and sub-mm-wave region optical measurement techniques are special qualified because of their high spatial resolution and bandwidth of up to 1 μm and 4 THz, respectively.[3] Here we show results of external electro-optic (EO) sampling with a $LiTaO_3$ crystal applied for the time-resolved field detection in TFMS lines.Very recently we also demonstrated the application of electric field-induced second-harmonic generation (EFISH) for internal probing of the electric field in the polymer layer of the waveguide.[4] With EFISH the Polymer itself serves as a EO transducer, based on a third-order nonlinear optical effect. This method exhibits non-invasiveness, however, with reduced sensitivity in comparison to EO-sampling.

The dielectric layer for the TFMS lines is cyclotene, a polymer with attractive material properties for high-speed interconnect systems (ε_r=2.7).[5] As substrate we use low-resistivity Si (5-8 Ωcm). A cyclotene film with 2.7 μm thickness is spin-deposited on a 700-nm-thick Al ground metalization under assistance of 3-aminopropyltriethoxysilane (3-APS) as adhesion promoter. The polymerisation takes place at 250°C in N_2 ambient. The 7.4-μm-wide signal conductor on top of the dielectric consists of a Ti/Au-layer with 20/680 μm thickness which provides good characteristics concerning adhesion, conductor losses and corrosion.

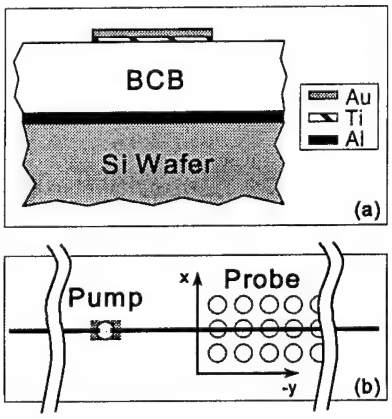

FIG.1. (a) Cross section and (b) topview of the TFMS line with internal PC-switch for impulsive measurement.

For time-domain measurements we use a mode-locked Ti:sapphire laser emitting 100 fs optical pulses with a repetition rate of 75.6 MHz. The setup is based on a pump probe scheme, where one pump pulse (10 mW average power) excites the 10V-biased-PC gap in the TFMSL and a temporarily delayed probe pulse is used for the detection of the propagating electric field with help of a $LiTaO_3$ EO transducer.

In order to reveal the characteristics of transmission line electric transients are probed at several positions in the y-direction along the line. The frequency-dependent

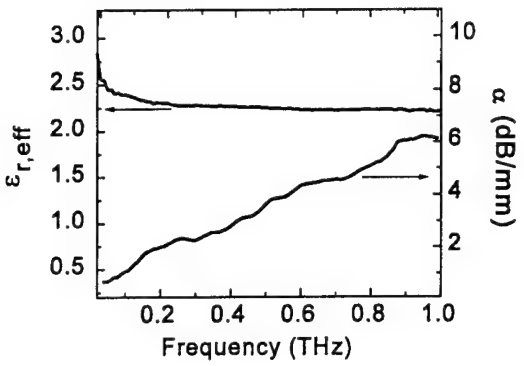

FIG.3. Experimentally determined attenuation and effective permittivity of the TFMS line in dependence of the frequency.

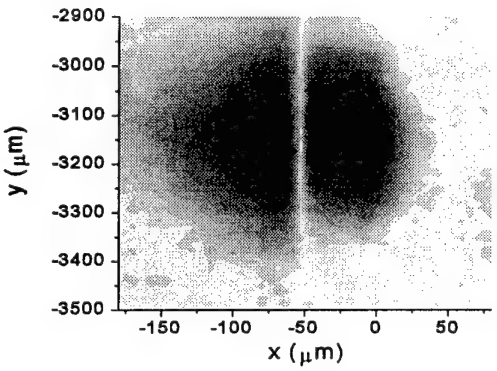

FIG.2. Spatial mapping of an electric ps-pulse transient on a TFMS line measured with EO sampling.

propagation constants are extracted out of the time-resolved measurements. The complex propagation constant $\gamma(f) = \alpha(f) + i \cdot \beta(f)$ with $\alpha(f)$ describing the attenuation and $\beta(f)$ the dispersion of the TFMS line are determined from Fourier transforms of the time-domain data. The effective permittivity $\varepsilon_{r,eff}(f)$ is calculated from $\beta(f)$ by $\varepsilon_{r,eff}(f) = (c \cdot \beta/2\pi f)^2$. Figure 2 shows the determined values of $\varepsilon_{r,eff}(f)$ and $\alpha(f)$. The high signal velocities of approx. 0,2 μm/ps are a result of the fairly low permittivity. $\varepsilon_{r,eff}(f)$ exhibits only a small dispersion over the hole mm- and sub-mm-regime. The attenuation is basically dominated by conductor ($\sim f^{1/2}$) and dielectric losses ($\sim f$). By increasing the polymer thickness with a concurrently broadening of the signal conductor, in order to maintain the desired impedance, α could be further reduced. However, for the sake of performance and packaging densities the polymer thickness should be kept sufficiently small.

The spatial field distribution of the guided signal propagating at 0.66 times of the vacuum light velocity is probed by EO mapping, shown in Fig. 3. This measurement is performed at a transmission line with a 9-μm-thick polymer and a 6-μm-wide signal conductor. The spatial mapping shows the magnitude of the electric field in normal direction to the signal conductor. The shown pulse has temporal width of 1.6 ps (FWHM). The spatial spread of the smallest measurable electric field amplitude reaches out to a distance of approx. 100 μm from the waveguide. These kind of measurements provide further important information on the cross-talk between neighboring waveguides and for design verification in general.

[1] J.-F. Luy, K. M. Strohm, H.-E. Sasse, A. Schüppen, J. Buechler, M. Wollitzer, A. Gruhle, F. Schäffler, U. Guettich, and A. Klaaßen, IEEE Trans. MTT, **43**, 4, 705-714 (1995)

[2] H.-M. Heiliger, M. Nagel, H. G. Roskos, H. Kurz, F. Schnieder, W. Heinrich, R. Hey and K. Ploog, Appl. Phys. Lett, **70,** 17, (1997)

[3] T. Pfeifer, H.-M. Heiliger, T. Löffler, C. Ohlhoff, C. Meyer, G. Lüpke, H. G. Roskos, and H. Kurz, IEEE J. Sel. Top. Quantum Electron. **2**, 586 (1996)

[4] M. Nagel, C. Meyer, H.-M. Heiliger, T. Dekorsy, and H. Kurz, R. Hey and K. Ploog, Appl. Phys. Lett. **72**, 9, (2 March 1998)

[5] P. B. Chinoy and J. Tajadod, IEEE Trans. Comp. Hybrids and Man. Techn. **16**, 7, 714-719, (1993)

TERAHERTZ RANGE ELECTRICAL GENERATION OF CURRENT OSCILLATIONS IN NANOSTRUCTURES

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This report summarize studies of the ballistic transport in nanostructures designed to produce carrier dispersion relation of a special kind. Namely, we deal with the dispersion relations having a differential negative effective mass in a some region of wave vectors [1]. Several different mechanisms of realization of such dispersion have been discussed and studied. They are: 1) hybridization of two electron dispersion relation with very different effective masses in an asymmetrical double quantum well or in a ΓX quantum well [2]; 2) mixing of the light and heavy hole states along the direction of uniaxial compression in diamond-like or zinc-blende-like semiconductor [3]; 3) mutual size quantization of the light and heavy holes in a heterostructure p-type quantum well [4,5,6].

We have demonstrated that a ballistic plasma of carriers with negative effective mass has no a stable stationary distribution of carrier concentration and electrostatic potential corresponding to a steady current, and a quasi-stationary oscillating current exists instead. The oscillation frequency is determined by a longitudinal mode of a self-tuning plasma cavity. It is in the subterahertz or terahertz ranges depending on a cavity length, which is of submicron range.

Traditional p-GaAs quantum wells of 10 nm width, 0.1÷1.0 μm length, $(0.2\div1.0)\times10^{11}$ cm^{-2} doping may be used to generate in the range of 0.25÷2.0 THz. At low temperatures and low voltages (below the optical phonon energy) ballistic transport condition is met in such structures.

To reach higher frequencies, very narrow quantum wells (up to 20 Å) and very short cavity length (up to 500÷300 Å) must be used. A narrow quantum well provide high energy and velocity of the holes with negative effective mass. Therefore we need to form a sufficiently deep hole quantum well. Very promising system for this implementation are InAs/InP and GaSb/InAlAs.

1. Z. S. Gribnikov, A. N. Korshak. Semiconductors, **28**, 1445 (1994).
2. Z. S. Gribnikov, A. N. Korshak, N. Z. Vagidov. J. Appl. Phys. **80**, 5799 (1996).
3. N. Z. Vagidov, Z. S. Gribnikov, A. N. Korshak. Semiconductors, **31**, 150 (1997).
4. A. N. Korshak, Z. S. Gribnikov, N. Z. Vagidov, S. I. Kozlovsky, V. V. Mitin. Phys. Stat. Sol. (b), **208**, 80 (1997).
5. V. V. Mitin, . Z. S. Gribnikov, A. N. Korshak, in *Physics of Semiconductor Devices,* eds. V. Kumar, S. K. Agarwal (Narosa Publ. House, New Delhi, India) pp. 134-141 (1998).
6. Z. S. Gribnikov, A. N. Korshak, N. Z. Vagidov, Z. M. Alexeeva. ICPS-23 Proc., Berlin, **4**, 3287 (1996).

Session 8: Optoelectronics

9: 00 **Receiver OEICs for Telecommunication Applications**
A. Scavennec, C. Gonzalez, G. Post *invited*
CNET, Bagneux France

9: 30 **Quantum Wire Laser on InP**
T. Schrimpf, P. Bönsch, D. Wüllner, H.-H. Wehmann, A. Schlachetzki
Technische Universität Carolo-Wilhelmina, Braunschweig Germany

9: 40 **High Power InGaAsP/GaAsP/AlGaAs Laserdiodes for 808 nm with a Low Mesa Structure**
A. Thies, F. Bugge, G. Erbert, A. Knauer, J. Maege, P. Ressel, R. Staske, K. Vogel, L. Weixelbaum, G. Tränkle
Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin Germany

9: 50 **InP Bulk Micromachined Tunable Bragg Mirrors for Optical Filter Applications in WDM systems**
J. Pfeiffer, R. Riemenschneider, J. Peerlings, A. Dehé, K. Mutamba, P. Meißner, H. L. Hartnagel
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10: 00 **Micromachining of Monolithic Fabry-Pèrot Filters in InP for WDM-Applications**
J. Daleiden, N. Chitica, S. Rapp, J. Bentell, B. Stalnacke
Royal Institute of Technology, Stockholm Sweden

10: 10 **All Epitaxial 1.55 µm Resonant Cavity Light-Emitting Diode Based on InP**
S. Rapp, F. Salomonsson, K. Streubel, M. Hammar, *J. Daleiden*
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10: 20 **Output Saturation Characteristics on InP/InGaAs Uni-Traveling-Carrier Photodiodes**
N. Shimiuzu, T. Furuta, T. Ishibashi
NTT System Electronics Laboratories, Kanagawa Japan

10: 30 **Optoelectronic Devices Based on Asymmetric Quantum-Well Heterostructures**
V. K. Kononenko
National Academy of Sciences of Belarus Belarus

Quantum Wire Laser on InP

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Recently low-dimensional semiconductor structures are intensely investigated for laser applications because of the expected improvements in threshold current, temperature stability, emission line-width, and dynamic behaviour. In contrast to zero-dimensional quantum-dots mainly fabricated by self-organized lattice-mismatched epitaxial growth, quantum wires (QWR) promise better controllability by anisotropic etching of V-grooves and anisotropic growth of QWRs in one step into the tip of the V-groove. This concept was demonstrated in the AlGaAs/GaAs system. However, the most promising material system for long-distance optical links is InGaAs(P)/InP.

Fig. 1 shows a schematic cross-section of a QWR laser-structure made of this material system. It consists of a layer stack which is grown in a first step and which comprises an InGaAsP waveguiding layer and a semi-insulating (s.i.) InP current-blocking layer. By patterning these layers by anisotropic wet-chemical etching through a Ti-mask its 3 µm window is transformed into the tip of a V-groove with a radius of curvature below 8 nm. Taking advantage of the anisotropic epitaxial growth from the metal-organic vapour phase (MOVPE) we deposited the InGaAs QWR into this tip. A second InGaAsP waveguiding layer follows as well as the Zn-doped InP top layer and the InGaAs contact layer also doped by Zn. The laser is completed by evaporating top and bottom ohmic contacts, mesa-etching, and cleaving of the mirrors.

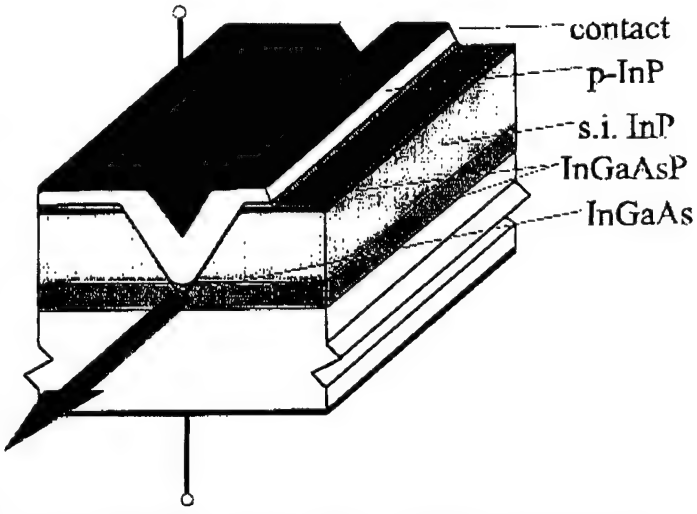

Fig. 1: Schematic cross-section of QWR laser on InP.

Fig. 2 shows the distribution of the hole current density through the QWR structure as calculated by the finite element method. Clearly visible is the current crowding at the upper edges of the V-

groove above the s.i. layer due to the extended contact mesa-structure. However, the highest current density is found – as desired – at the QWR location in the tip of the V-groove. We also calculated the distribution of the optical field and found a pronounced increase of its overlap with the QWR by introducing the two waveguiding quaternary layers with a bandgap equivalent to 1.2 µm wavelength.

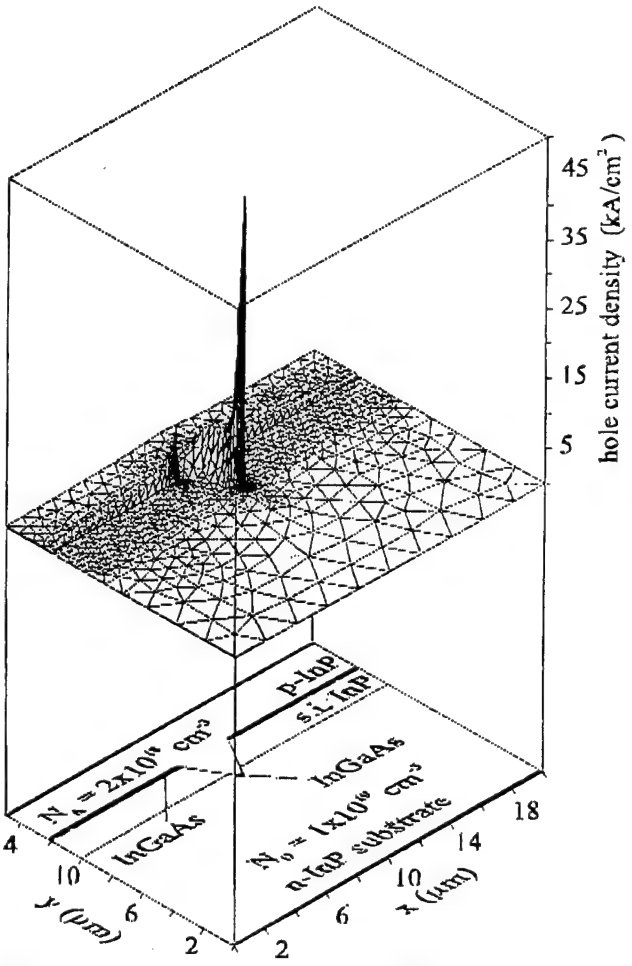

Fig. 2: Calculated hole current density through the QWR structure.

For the patterning of the V-groove we employed a two-step wet-chemical etching process which was first optimized with InP. The resulting tip radii and roughnesses were characterized by atomic force microscopy (AFM). The MOVPE-growth parameters were chosen such that the anisotropy of the quaternary and ternary layers is enhanced whereas InP is grown almost isotropically in order to cover the structure as homogeneously as possible. The growth rates on the respective planes were determined with thicker layers. The composition of the ternary and quaternary layers depends on the geometry and the orientation of the underlying planes. This is discussed on the basis of energy-dispersive X-ray and photoluminescence (PL) measurements of the active ternary layer.

The geometry of QWRs is determined by AFM on material-selectively etched cross-sections. It depends on the growth temperature and the thickness of the underlying InP buffer layer, which has been found to improve the PL intensity and its line-width.

High power InGaAsP/GaAsP/AlGaAs laserdiodes for 808 nm with a low mesa structure

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Abstract:

High power wide aperture lasers are important for a wide variety of applications including diode-pumped solid state lasers, direct diode materials processing and thermal printing. Most high power wide aperture lasers and diode laser bars use an oxide- or implant confined structure. We developed a low-mesa structure to improve the current and optical confinement and suppress the generation of whispering gallery modes.

Fig. 1 shows a schematic of the laser structure, grown by low pressure MOCVD. The Al-free active region consists of a strain-compensated InGaAsP/GaAsP quantum well. The active region is embedded into AlGaAs waveguide and cladding layers, forming a LOC-structure. The cladding and waveguide layers consist of $Al_{0.7}Ga_{0.3}As$ and $Al_{0.65}Ga_{0.35}As$, respectively. The fundamental parameters of our epitaxial structures measured under pulsed conditions for 100 µm x 1000 µm uncoated devices are: $j_{th} = 250$ A/cm^2 (threshold current density); $\eta_i = 92$ % (internal quantum efficiency); $\alpha_i = 1.3$ cm^{-1} (internal losses); $\theta_\perp = 28°$ (vertical farfield).

Process technology for the fabrication of the low mesa structure starts with wet chemical etching of the contact and cladding layers to define the low mesa. The deposition of a 50 nm thick Si_3N_4-layer for insulation in a self-aligned process follows, using the first resist mask for the lift off. Single diode lasers have a Ti/Pt/Au p-contact with 3 µm electroplated Au for heat spreading, while the laser bars have a He^+-implanted facet region using a first Ti/Pt/Au p-metallisation for masking, followed by a second Ti/Pt/Au metallisation. In a subsequent backside process the wafers were thinned down to 120 µm followed by an evaporation of the ohmic backside contact. Rapid thermal annealing for contact formation finishes wafer processing. Antireflection (5 % ... 30 %, depending on resonator length) and high reflection (95 %) coatings are deposited on the laser facets, after cleaving into bars. The processing of the bars leads to an excellent homogeneity. In Fig. 2 is shown the output power distribution of the single stripes of an unmounted laser bar. The variation is smaller than 5 %.

Single stripe diodes are soldered p-up on copper heatsinks to facilitate measurements under cw-conditions. Fig. 3 shows the power current voltage characteristic of a single laserdiode with a stripe width of 100 µm and a resonator length of 2000 µm. A maximum output power of 5.2 W with a differential quantum efficiency of 1.17 W/A and a serial resistance of 80 mΩ was achieved. The lifetimes of diodes from this material at a constant optical output power of 1.5 W and a temperature of 25°C were tested for 1000 h. The diodes degrade with a rate of 1.3×10^{-5}/h.

As shown in Fig. 4, we get from 10 mm laser bars with a fill factor of 30 % consisting of 48 diodes and a resonator length of 600 µm an output power of more than 60 W at a current of 90 A and a conversion efficiency of 42 %. Studies concerning lifetimes of these bars are under progress.

This work was sponsored by the „Laser 2000" project of the German BMBF and the project HOLLAR of the Freistaat Thüringen. The laser bars were mounted at Jenoptik Laserdiode.

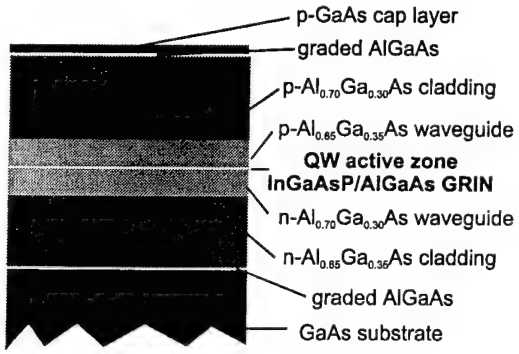

Fig. 1: Schematic of the laser structure

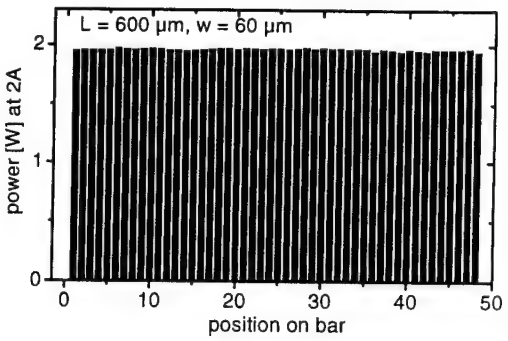

Fig. 2: Homogeneity in output power of a 10 mm laser bar with 48 diodes

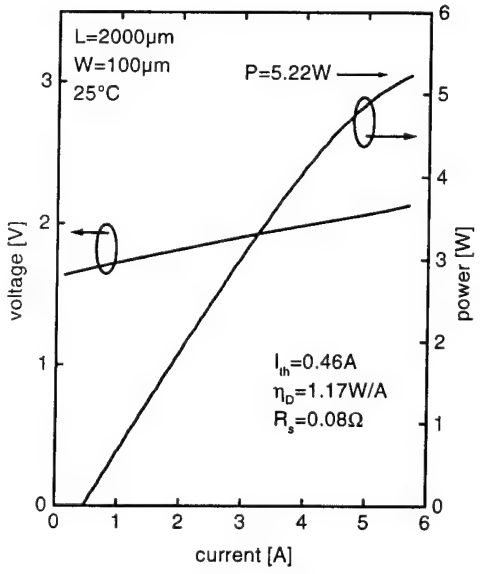

Fig. 3: CW power current voltage characteristic of a 100 µm x 2000 µm single laserdiode

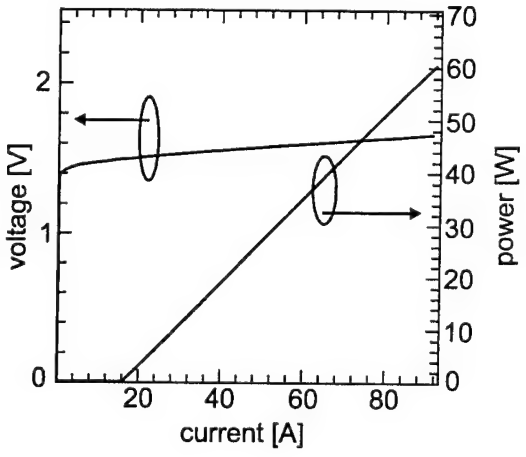

Fig. 4: CW power current voltage characteristic of a 10 mm laser bar with 48 diodes

InP bulk micromachined tunable Bragg mirrors for optical filter applications in WDM systems

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Abstract

Many recent research activities in MOEMS (micro optoelectro mechanical systems) are focused on the fabrication of low cost and high performance Fabry-Pérot filter applications for WDM sytems (wavelength division multiplexing) at wavelengths around 1550 nm [1].
The optical performance of these devices strongly depends on the controlled micromechanical displacement of the movable part of the filter during actuation. The need of high selectivity finally leads to an increase of both, mirror reflectivity [2] and resonator length [3]. This mainly affects the tunability properties of the micro structures, which is due to the amplification of internal stress relaxation within the necessary quarter wavelength multilayer stack.
We developed an InP-based bulkmicromachining technology for tunable optical filters using released multilayer membranes.

Filter Design and Fabrication

The concept bases on a physically separation of the filter movable component integrated on the chip and the static mirror on top of a GRIN-lense as indicated in figure 1. This implies the following advantages:

- inherent flatness of the static mirror
- direct coupling of the incident light into the Fabry-Pérot filter
- backside illumination of the tunable mirror (simplifies the integration of a photodetector on top of the epitaxial Bragg mirror)

The tunable Bragg mirror is defined by a stack of 20.5 pairs InGaAs/InAlAs epitaxial layers grown lattice matched to an InP substrate. The additional thickness of the membrane is about 4.6 µm.

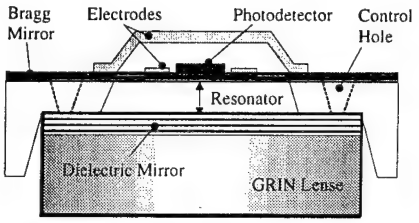

Fig. 1: Cross-section of an electrostatically tunable Fabry-Pérot Filter

We introduced the thermal actuator principle, using NiCr resistors on top of the membrane suspension as well as electrostatical actuation by an air bridge electrode configuration. The definition and release of membrane structures by highly selective wet-etching technology is the basis of an optimized symmetrical alignement of front and backside processing. Large area free-standing membranes with diameters varying from 300 - 1100 µm are fabricated.

The structural analysis of mechanical filter properties using the FEM program ANSYS enables calculations of different stiffness ratios for membrane and suspension [4]. An optimzed geometry for 1mm^2 mirrors has been found out and realized, using suspension beams of 50µm x 800 µm [Fig. 2].

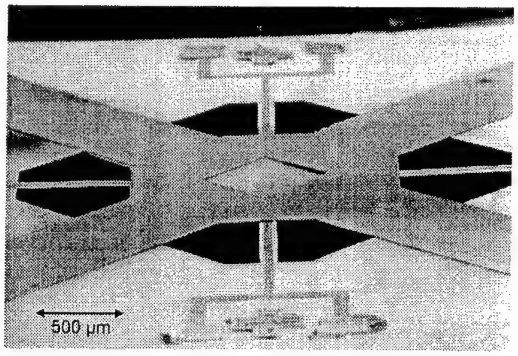

Fig. 2: Free-standing Bragg mirror (1.2 mm^2) covered by an Au-airbridge for electrostatical actuation

A further reduction of beam stiffness can be achieved, if defined thinning of the beam thickness is possible.

Mechanical Characterization

In order to reduce optical absorption losses, a sufficient doping concentration of the InGaAs-layers is necessary. An additional deposition of dielectric layers onto the conductive multilayer stack will be stringent to enable a sufficient isolation between actuator and photodetector. The influence of additional SiO_2 coatings onto InGaAs/InAlAs-mirrors has been studied and it was found to be a reliable technology for compensating the residual stress in a floating membrane [5]. The compensation of epitaxial built-in stress is possible with low film thicknesses (180 ... 250 nm).

The characterization of built-in stress in heteroepitaxial multilayer stacks caused by differing lattice constants and thermal expansion coefficients of epitaxial layer materials is essential for the micromechanical optimization of the mirror devices. The average internal stress and the stress gradient within the multilayer stack is analyzed qualitatively for varying growth conditions, changing the stress profile from tension to compression. The characterization showed that the radius of curvature of cantilever test structures can be increased from 9.6 mm up to 41mm. Together with a careful choice of beam geometry it is possible to fabricate almost plane membranes using pre-stressed grown epitaxial layers. The maximum center deflection of the mirror plate (diameter 1 mm^2) is less than 40 nm.

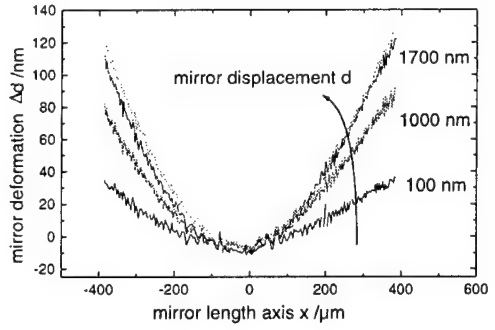

Fig. 3: Actuation induced deformation of thermal actuated mirror

Besides the inherent deformation of membrane structures due to the stress relaxation after the release of the epitaxial layer, an additional amount of bending occurs while tuning the mirrors. The tuning performance has been studied for the thermal actuator. The effect of gradual temperature distribution within the suspension, leads to a bimorph expansion of the multilayer in the regions of heat generation.

The maximum center displacement of the mirror plate observed by interferometric measurement was about 1.7 µm. This would correspond to a tuning range of more than two times the free spectral range (tuning range about 775 nm) for the long cavity resonator concept. A sufficient displacement is achieved for an actuation power of 250 mW.

In Fig.3 the bending profiles for different states of displacement are compared. Discussing the center region of the mirrors (diameter less than 400µm) the actuation induced bending is restricted to values of less than 40 nm.

Conclusion

We have presented concepts for tunable Fabry-Pérot filter devices, being an important component of optical communication systems. An InP- based bulk micromachining technology is developed for both, thermal and electrostatic actuation principles. Mechanical characterization sufficient reduction of the membrane bending after fabrication and during membrane actuation.

Acknowledgement

We would like to thank the European Union under ESPRIT project No. 22687 for financial support.

References

[1] A. T. T. D. Tran, Y. H. Lo, Z. H. Zhu, D.Haronian, E. Mozdy, IEEE Photonics Technology Letters, Vol. 8, No. 3, (1996)

[2] F. S. Choa, K. Tai, W. T. Tsang, S. N. G. Chu, Appl. Phys. Lett., **59**, 2820, (1991)

[3] J. Peerlings, A. Dehé, A. Vogt, M. Tilsch, C. Hebeler, F. Langenhan, P. Meissner, Proc. Eurosensors XI, Warsaw, Sept 21-24, pp. 1353-1356

[4] K. Mutamba, J.Pfeiffer, J.Peerlings, R.Riemenschneider, A. Vogt, A. Dehé, M. Brauch, B. Meister, N. Dragojevic, P. Meissner, H.L. Hartnagel, ITMPE '97, Okt 14-17 1997, Beijing, China

[5] R. Riemenschneider, J. Peerlings, J. Pfeiffer, A. Dehé, A. Vogt, P. Meissner, H.L. Hartnagel, SPIE Photonics West '98, San Jose, USA

Micromachining of monolithic Fabry-Pérot Filters in InP for WDM-Applications

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Monolithically integrated tunable Fabry-Pérot Filters and photodetectors based on InP are of increasing interest for high-density wavelength division multiplex (WDM) fiber-optic transmission. For this application filters with narrow bandwidth and high selectivity are needed since the channel spacing is designed to 1.6 nm or even 0.8 nm [1]. In addition a continuous wavelength tuning of $\Delta\lambda = 40$ nm is required.

In the last years considerable progress in the field of GaAs-based micro opto-electro-mechanical systems (MOEMS) has been made [2,3]. However, there are only a few publications on InP-based MOEMS [4,5].

Recently, we have presented an InP-based optical filter with a full width at half maximum (FWHM) less than 0.3 nm [6] as well as an optically pumped air gap vertical cavity surface emitting laser (VCSEL) with a linewidth of 0.15 nm [7]. In the present work we show an enhanced tunability of the vertical cavity obtained through electrostatic actuation of a movable membrane.

The filter-structure was grown on n-InP substrate by MOCVD. Two high reflectivity (R>99.7%) Bragg mirrors define the Fabry-Pérot cavity (Figure 1). The lower mirror consists of three pairs of InP and InGaAs layers. The sacrificial InGaAs layers have an optical thickness of $\lambda/4$ ($\lambda = 1550$ nm) while the InP-layers are $3/4\lambda$ thick in order to improve the mechanical stability. A twelve period $\lambda/4$ dielectric Si_3N_4/SiO_2 stack acts as the top mirror. The air gap cavity has a length of λ and the movable membrane is $9/4\ \lambda$ thick. Both cavity and bottom mirror are fabricated by the combination of non-selective dry etching and high selective wet etching of the sacrificial InGaAs. Figure 2 shows a SEM micrograph of a freestanding movable membrane suspended by 4 beams. By reverse biasing the p-doped membrane and the n-doped substrate an electrostatic force bends the membrane downwards hence decreasing the cavity length.

Depending on the geometry of the structures (Figure 1, left) the membranes could be actuated between $\Delta\lambda = 5$ nm ($L = 80\ \mu m$, $s = 0\ \mu m$) and $\Delta\lambda = 37$ nm ($L = 170\ \mu m$, $s = 20\ \mu m$) with a voltage of 17 V.

Further investigations will emphasize on the monolithic integration of a photodetector with the filter described above.

References:

[1] C.D. Chaffee, "Telecoms mix wavelenghtes to boost markets." Photonics Spectra, Aug. pp. 393-395, 1996.

[2] J. Peerlings et al., "Long resonator micromachined tunable GaAs/AlAs Fabry-Pérot filter", IEEE Photonic Technol. Lett., 9 (1997) pp. 1235-1237.

[3] M.C. Larson et al., IEEE Photon. Technol. Lett. 7 (1995) 382.

[4] R. Riemenschneider et al., "Mechanical-Optical Analysis of InP-based Bragg Membranes for Selective Tunable WDM Receivers", SPIE Photonic West 98, Vol. 3276 (1998) San Jose CA, USA.

[5] C. Seassal et al., "Micromachined Structures For Vertical Microelectrooptical Devices on InP, Proceedings of the IPRM'96, p. 275-278.

[6] N. Chitica, K. Streubel, J. Andre, "Tunable Monolithic Fabry-Perot Filter Manufactured by Selective Etching of InGaAs/InP Epitaxial Films", Proceedings of the IPRM'97, p. 115-117.

[7] K.Streubel, S.Rapp, J.André and N.Citica, Fabricationof InP/Air-gap Distributed Bragg Reflectors and Micro-Cavities, J. Mat. Sci. Eng. B 44 (1997), p. 364-367.

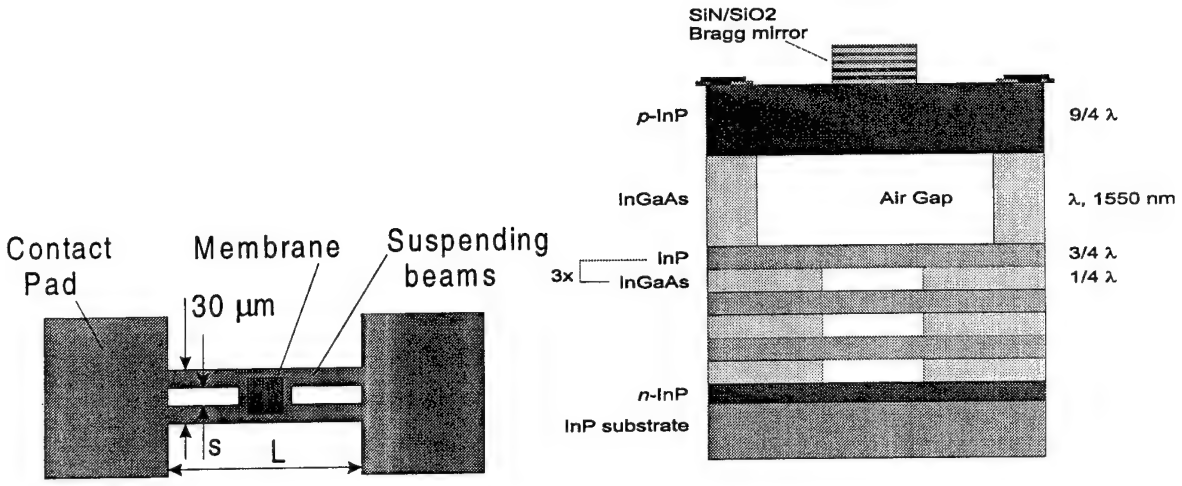

Figure 1: Schematic of a micromechanically tunable Fabry-Pérot filter, left: top view, right: cross section.

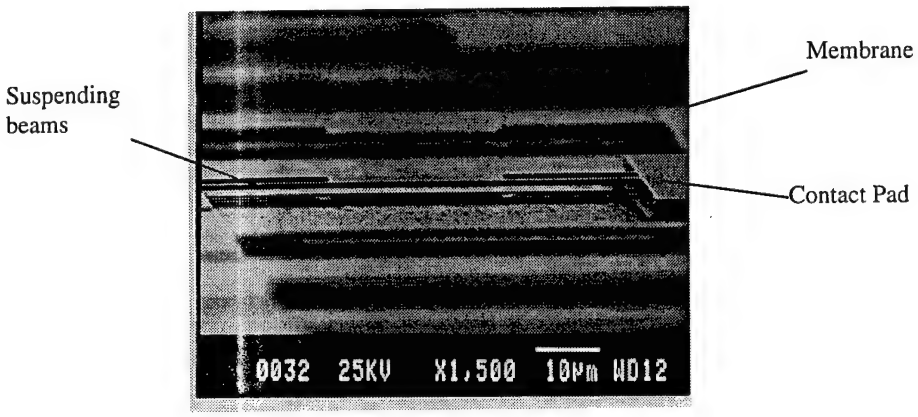

Figure 2: SEM micrograph of a freestanding movable membrane suspended by 4 beams.

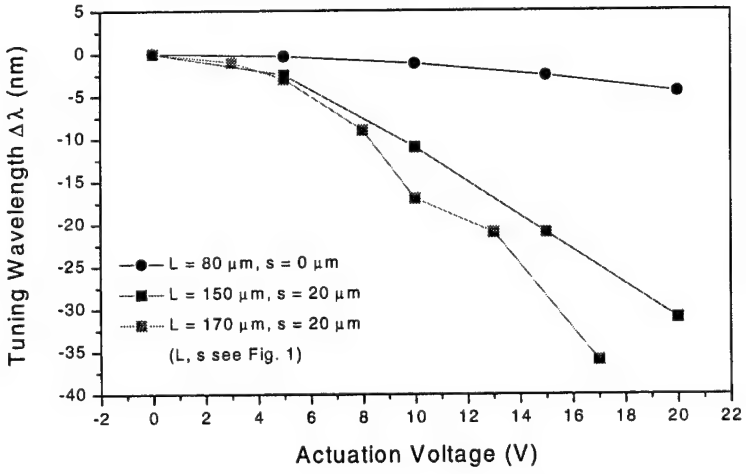

Figure 3: Tuning characteristics for structures with different geometries.

All Epitaxial 1.55μm Resonant Cavity Light-Emitting Diode Based on InP

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Abstract

Resonant cavity light emitting diodes (RCLEDs) for applications within telecommunications have gained interest due to their superiority to ordinary LEDs. For short and medium distance transmission they are competing with vertical cavity lasers (VCSELs) because of their low cost fabrication as well as their comparable high reliability. The resonant cavity introduces an enhancement of the spontaneous emission life time and rate, thus reducing the emission line width. This leads to an increase in the transmission distance in optical fibres due to reduced chromatic dispersion. Furthermore, the RCLED design improves other characteristics drastically, such as increased modulation bandwidth and facilitated fibre coupling. For short wavelength RCLEDs, considerable progress has been made during recent time[1]. As known from the VCSEL devices[2,3], achieving similar results at long wavelength is much more difficult. This is implied by the enhanced optical loss at long wavelength, such as non-radiative recombination as well as due to the lack of materials exhibiting a high refractive index contrast. For this reason, Bragg reflectors made up by GaInAsP and InP consist of 50 pairs of layers in order to achieve a reflectivity beyond 99%. 1.55μm RCLEDs fabricated so far use one metallic mirror and an epitaxial output mirror of only 12 periods[4] or dielectric top mirrors[5]. In the present work, we have replaced the metal mirror by a highly reflective InP-based mirror. We fabricated an all epitaxial 1.55μm RCLED based on two InP/GaInAsP mirrors grown by metal organic vapour phase epitaxy (MOVPE). The structure (see Figure 1) is consisting of an 8 period p-doped (Zn) top mirror, a 50 period n-doped (Si) bottom mirror and 9QW GaInAsP-active material. Mesas are fabricated using a dry etching procedure for the top mirror. Followed by a regrowth step with semi-insulating InP:Fe for better thermal performance. The current is injected via a contact ring on top of the mesa structure. Figure 2 shows the reflectivity spectrum of the finished structure, where the cavity mode can be seen clearly. Electrically pumped, the spectrum looks as shown in Figure 3. The emission line width is 9.5nm, compared to 40nm line width of the photoluminescence of the quantum wells without cavity. For a 36μm diameter device, the output power into a cleaved multi mode fibre starts to saturate at about 20mA where it is 3μW. Improved current injection promises a further increase in terms of output power. Also, the p-doping levels of the top mirror have to be optimised to achieve better performance of the device.

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[1] H. De Neve, J. Bolondelle, R. Baets, P. Demeester, P. Van Daele, and G. Borghs, *Photonics Technology Letters 7*, 287 (1995)

[2] D. Babic, K. Streubel, R.P. Mirin, N.M. Magalit, J.E.Bowers, E.L. Hu, D.E. Mars, Long Yang, and K. Carey, *IEEE Photonics Technology Letters 7*, 1225 (1995)

[3] K. Streubel, S. Rapp, J. André, and J. Wallin, *IEEE Photonics Technology Letters 8*, 1121 (1996)

[4] B. Depreter, J. Bolondelle, I. Moerman, R. Baets, P. Van Daele, P. Demeester, *Proceedings on IEEE Laser Electro-Optics Society Annual meeting (LEO'97), San Francisco , USA, 11-13 Nov 1997*, p. 241

[5] G.L. Christenson, A.T.T.D. Tran, Z.H. Zhu, Y.H. Lo, M. Hong, J.P. Mannaerts, and R. Bhat, *IEEE Photonics Technology Letters 9*, 725 (1997)

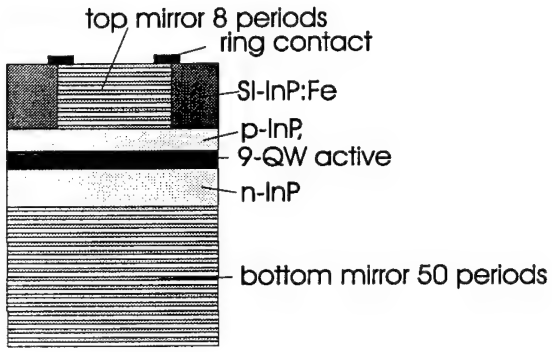

Figure 1: RCLED structure

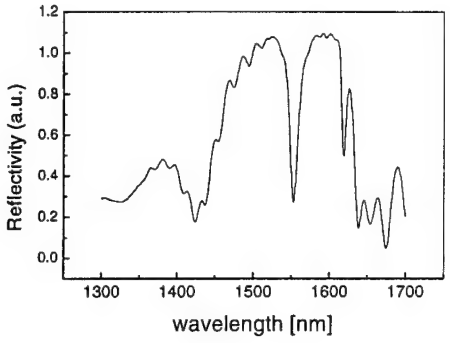

Figure 2: Spectral reflectivity of the RCLED structure

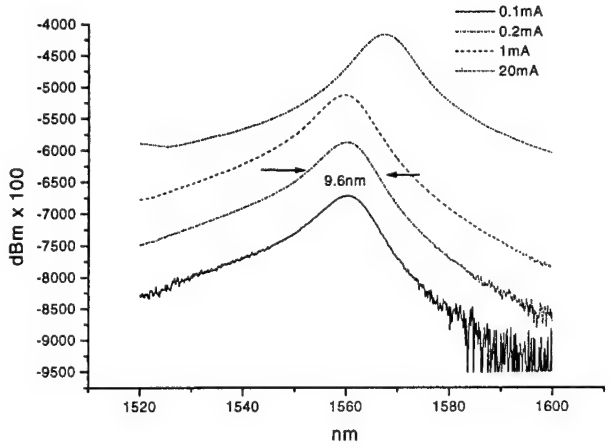

Figure 3: Spectra for different currents

22nd Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE '98) May 24-27, 1998, Zeuthen, Germany

Output Saturation Characteristics of InP/InGaAs Uni-Traveling-Carrier Photodiodes

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Because of its operating mode, in which only electrons are used as active carriers and electron velocity overshoot reduces the space charge in the diode depletion layer, the uni-traveling-carrier photodiode (UTC-PD) can drive much higher current densities than a conventional pin photodiode while maintaining a broad bandwidth.[1],[2],[3] This feature, combined with optical amplification, allows us to realize high output and ultrahigh-speed optical to electric signal conversion. In this paper, we show the temporal photoresponse characterization of InP/InGaAs UTC-PDs and discuss the output saturation mechanism.

We fabricated UTC-PDs in an InP/InGaAs epitaxial structure grown by MO-VPE on a semi-insulating InP substrate.(Fig. 1) The PD device, with back illuminated geometry (20 μm^2 junction area), is integrated with coplanar waveguides where the anode is connected to two 50-Ohm signal lines. Photoresponse of the device to a 1.55 μm incident pulse (FWHM = 790 fs) was measured using an electro-optic sampling (EOS) technique.

Typical output waveforms with an optical input power P_{in} as a parameter are shown in Fig. 2 for bias voltages of - 0.5 V and - 5 V. At V_{bias} = - 5 V, the output peak intensity I_P increases monotonically with an input in the measured range. Here, however, when the P_{in} increases from 1.28 to 2.1 pJ/pulse, weak output saturation is seen accompanied with an FWHM widening from 3.1 to 3.9 ps (corresponding f_{3dB} variation from 100 to 80 GHz). On the other hand, at V_{bias} = - 0.5 V, significant I_P saturation appears. Since the operating voltages are not deeply positive at this bias, the observed saturation is not due to diode forward current. It is also found that the rise time remains at 1.1 ps (20%-80%) for all the curves and the saturation occurs very sharply with input level. These findings indicate that a constant charge injected into the carrier collection layer switches the current conduction from a normal to a saturation phase. Such a behavior is peculiar to the space charge limited current mechanism and the band profile of the collection layer can be mostly flattened on the absorption layer side.

Saturation currents I_{Psat} determined at various biases are shown in Fig. 3 as a function of diode operating voltage V_{op}. For a V_{op} of smaller than 1 V, a gradient of I_{Psat} vs. V_{op} can be explained by assuming electron velocity with overshoot, $v_e \approx 4 \times 10^7$ cm/s. For a V_{op} beyond 1 V, the overshoot effect tends to be less significant, leading to a more gradual increase in I_{Psat}. The curve also indicates that the device can function even at zero bias voltage.

In the present device, I_{Psat} reaches 400 kA/cm² (80 mA for a 20 μm^2 area device), which is roughly one order of magnitude greater than that for a conventional pin-PD and high enough to directly drive, for example, ultrahigh-speed SCFL-based integrated circuits and electro-absorption optical modulators.[4],[5]

[1] T. Ishibashi, N. Shimizu, S. Kodama, H. Ito, T. Nagatsuma, and T. Furuta, "Uni-Traveling Carrier Photodiodes," Tech. Dig. Ultrafast Electronics and Optoelectronics (OSA Spring Topical Meeting), p. 166/UWA2-1, 1997.
[2] N. Shimizu, N. Watanabe, T. Furuta, and T. Ishibashi, "High-Speed InP/InGaAs Uni-Traveling-Carrier Photodiodes," 55th Annual Device Research Conference, p. 164, 1997.
[3] T. Ishibashi, S. Kodama, N. Shimizu, and T. Furuta, "High-Speed Response of Uni-Traveling Carrier Photodiodes," Jpn. J. Appl. Phys. Vol. 36, p. 6263, 1997.
[4] M. Miyamoto, M. Yoneyama, K. Hagimoto, T. Ishibashi, and N. Shimizu, "Ultra High Speed Optical Receiver with Uni-Traveling Carrier Photodiode acting as a Logic IC Driver," CLEO/Pacific Rim '97, PD2, p. 11, 1997.
[5] M. Yoneyama, A. Hirano, Y. Miyamoto, K. Hagimoto, N. Shimizu, T. Ishibashi, and K. Wakita, "A 40-Gbit/s Demultiplexer using an Optical Modulator Driven by a Uni-Traveling-Carrier Photodiode," to be presented at IEICE spring meeting, March, 1998.

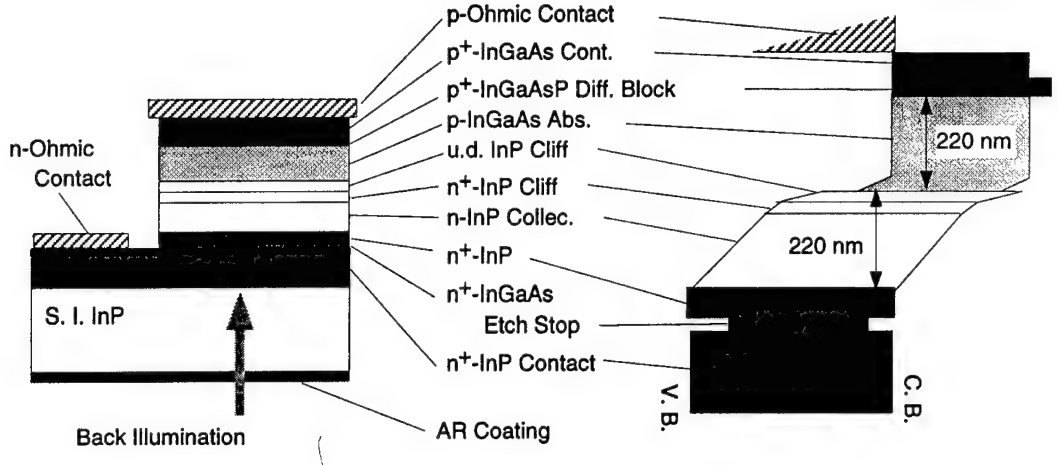

Fig. 1 MO-VPE grown InP/InGaAs UTC-PD structure.

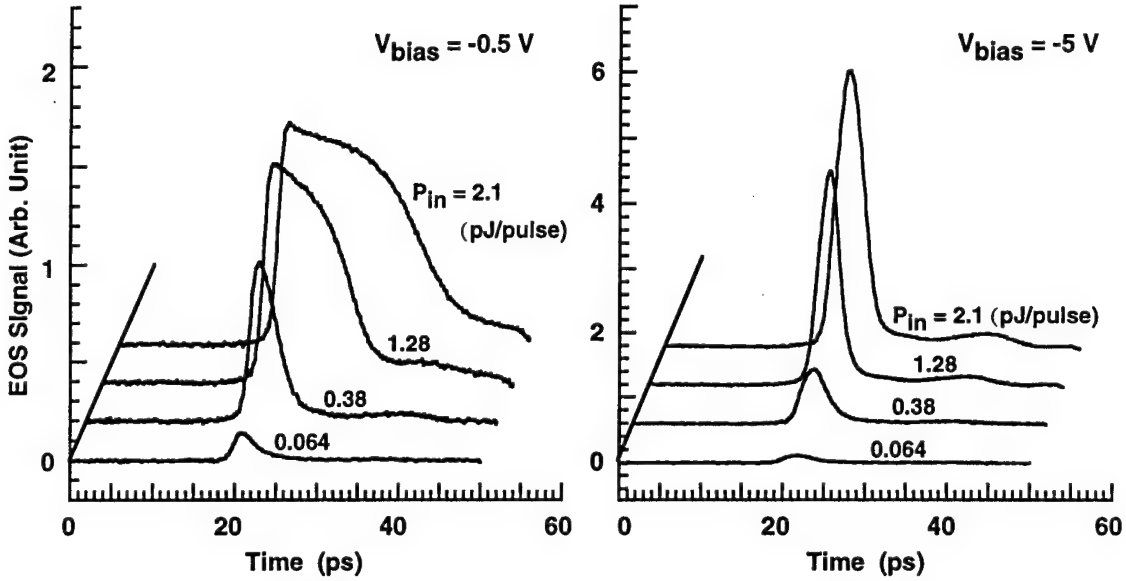

Fig. 2 Photoresponse waveforms of a UTC-PD with optical input level as a parameter (Incident pulse: λ = 1.55 μm, FWHM = 790 fs).

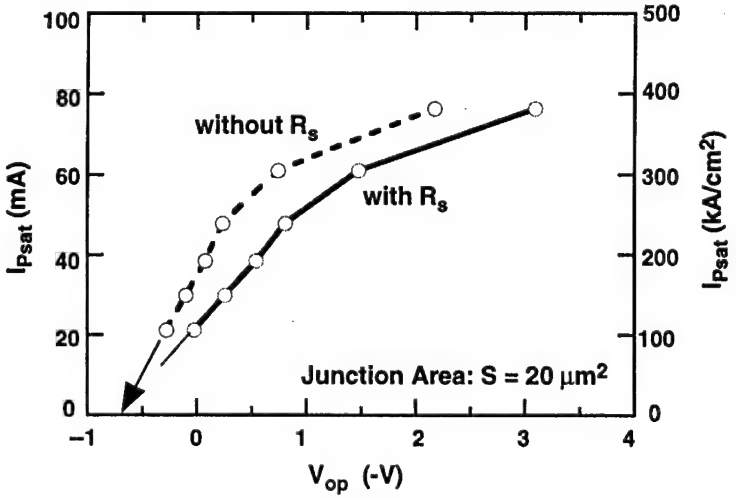

Fig. 3 Saturation current of photoresponse vs. diode operating voltage

OPTOELECTRONIC DEVICES BASED ON ASYMMETRIC QUANTUM-WELL HETEROSTRUCTURES

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Use of asymmetric quantum-well heterostructures is a new conception of band-gap engineering for semiconductor electronics. In this manner there are developed solid state photomultipliers, infra-red detectors, optical modulators, polarization insensitive light amplifiers, bistable laser diodes, and other modern semiconductor nanodevices.

Results of study of dynamic and spectral characteristics of a novel type of injection lasers based on asymmetric quantum-well heterostructures with active regions of different widths and/or compositions are presented. Due to asymmetric quantum-well heterostructures new possibilities to control spectral, power, and temporal properties of laser diodes and to widen functionality of optoelectronic devices are opened up. For this type heterostructures, wide-band gap barrier layers separating different quantum wells may be with a linear or parabolic energy potential profile. In addition, an arrangement of active regions relative to n- and p-type wide-band gap emitters determines definite conditions of current carrier injection into different quantum wells. Conditions for nonuniform excitation of the quantum wells are also provided by a suitable modification of the energy potential profile in the barrier regions due to their compositions, widths, and doping. Application of quantum wells with varying widths and/or compositions gives an additional degree of freedom for the band-gap engineering to stipulate required regimes of the device operation.

For asymmetric quantum-well heterostructure laser diodes, possible operation regimes are analyzed in detail and optimal schemes of the band gap energy diagrams are proposed. Depending on the composition of the material of quantum-wells and emitter barriers and their widths, the Q-factor of the cavity, and the pump current, effects of spectral and power switching [1, 2] and also of regular pulse generation at single, two, or three remote wavelengths [3] are described. Because of electron-optical interaction between different

quantum wells, radiation pulses at far remote lasing wavelengths occur to be locking. By choice of the pump current and cavity Q-factor it is able to control an amplitude, repetition rate, and duration of regular light pulses.

Calculations, based on rate equations, were made for the AlGaAs compound laser systems. In the effective mass approximation, optical transitions involving the subband levels of heavy and light holes have been taken into account and a change in the polarization factor versus light frequency has been included. Asymmetric heterostructure waveguide properties have been considered too, and the nonlinear electron-optical connection between the quantum wells, which results in weak confinement of radiation propagating the whole the active regions, is analyzed. The synchronization behaviour of coupled quantum wells due to injection efficiency oscillations in these systems is described.

New ideas are developed to realize laser diode sources with expanded discrete or continuous emission spectra. Mechanisms of spectral broadening and a role of gain suppression are discussed. The sources based on asymmetric quantum-well heterostructures are partially attractive for special applications such as bistable elements [4] and clock-pulse generators [5] at high-speed optoelectronic devices. The novel laser and amplifier elements with a broad-band tunable spectrum [6, 7] can be used in spectroscopy or metrology and for multi-chanel fiber optical regenerators or as pump sources of solid-state lasers.

References

1. V.K. Kononenko. Proc. SPIE. Vol.1724, *Tunable Diode Laser Applications.* 1992. P.89-101.

2. A.A. Afonenko, V.K. Kononenko, and I.S. Manak. Tech. Phys. Lett. 1993. Vol.19, No.9. P.35-39.

3. A.A. Afonenko, V.K. Kononenko, and I.S. Manak. Proc. SPIE. Vol.2749, *Photonic Component Engineering and Applications.* 1996. P.2-10.

4. V.K. Kononenko, A.A. Afonenko, and I.S. Manak. Bistable Semiconductor Laser Element. Patent BY, No.1099 (31 Dec. 1993).

5. A.A. Afonenko, V.K. Kononenko, and I.S. Manak. Semiconductor Laser. Patent BY, No.1385 (1 July 1994).

6. V.K. Kononenko and S.A. Lomashevich. Semiconductor Light Amplifier. Patent RU, No.2062543 (1 July 1991).

7. V.K. Kononenko, I.S. Manak, S.V. Nalivko, V.A. Shevtsov, and D.S. Shulyaev. J. Appl. Spectrosc. 1997. Vol.64, No.2. P.234-241.

Session 9: III/V Nitride Devices

11: 10	**Present and Future of Group III-Nitride Semiconductors** *I. Akasaki,* H. Amano, Meijo University, Nagoya	*invited* Japan
11: 40	**Processing Challenges for GaN-Based Electronic and Photonic Devices** *S. J. Pearton* University of Florida, Gainesville	*invited* USA
12: 10	**AlGaN/GaN - HEMT's for High Power Microwave Amplifiers** K. Chu, B. Green, *L. F. Eastman* Cornell University, Ithaca	 USA
12: 20	**Technology and Electrical Characterization of AlGaN/GaN HFET's** *I. Daumiller,* C. Kirchner, M. Kamp, K. J. Ebeling, E. Kohn University of Ulm	 Germany
12: 30	**Thermal Simulation of High Power GaN Microwave MODFETs** *N. G. Weimann,* L. F. Eastman Cornell University, Ithaca	 USA
12: 40	**Thermally Stable GaN-Based Field Effect Transistors** W. Rieger, J. Hilsenbeck, E. Nebauer, A. Abrosimova, J. Würfl, G. Tränkle Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin	 Germany

PROCESSING CHALLENGES FOR GaN-BASED ELECTRONIC AND PHOTONIC DEVICES

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ABSTRACT

Recent progress in the development of dry and wet etching techniques, implant doping and isolation, thermal processing, gate insulator technology and high reliability contacts is reviewed. Etch selectivities up to 10 for InN over AlN are possible in Inductively Coupled Plasmas using a Cl_2/Ar chemistry, but in general selectivities for each binary nitride relative to each other are low (≤2) because of the high ion energies needed to initiate etching. Improved n-type ohmic contact resistances are obtained by selective area Si^+ implantation followed by very high temperature (>1300°C) anneals in which the thermal budget is minimized and AlN encapsulation prevents GaN surface decomposition. Implant isolation is effective in GaN, AlGaN and AlInN, but marginal in InGaN. Candidate gate insulators for GaN include AlN, AlON and Ga(Gd)O_X, but interface state densities are still to high to realize state-of-the-art MIS devices.

INTRODUCTION

Current GaN-based device technologies include light-emitting diodes (LEDs), laser diodes and UV detectors on the photonic side and microwave power and ultra-high power switches on the electronics side. The LED technology is by now relatively mature, with lifetimes of blue and green emitters apparently determined mostly by light-induced degradation of the polymer package that encapsulates the devices. The main trends in this technology appear to be optimization of optical output efficiency and solving the polymer package degradation issue. For the laser diodes one of the main lifetime limiters was p-ohmic metal migration along dislocations to short out the GaN p-contact layer by spiking all the way to the n-side of the junction. This is exacerbated by the generally high specific contact resistance (R_C) of the p-ohmic contact and the associated heating of this area during device operation. The advent of lower threshold devices and the dislocation-free GaN overgrowth of SiO_2 masked regions has allowed achievement of laser lifetimes over 10,000 hours. Facet formation on the laser has been achieved by dry etching, cleaving, polishing and selective/crystallographic growth. In structures grown on Al_2O_3 both contacts must be made on the top of the device and hence dry etching is necessary to expose the n-side of the junction. Fabrication of UV detectors is relatively straightforward and the main issue seems to be one of improving material purity and quality.

For electronic devices for microwave power applications, the main process improvements are needed in the areas of low R_C n-ohmic contacts (the requirements are more stringent than for photonic devices, with $R_C \leq 10^{-7}\Omega cm^{-2}$ being desirable), stable and reproducible Schottky contacts, and low damage dry etching that maintains surface stoichiometry. For the proposed

high power switches (capable of 25 kA with 3kV voltage stand-off) there are a number of possible device structures, including thyristors and several types of power MOSFET. A schematic of the latter is shown in Figure 1. In this case, critical technologies include high implant activation efficiency, gate insulator, trench etching for capacitor formation and high temperature/high current stable ohmic contacts.

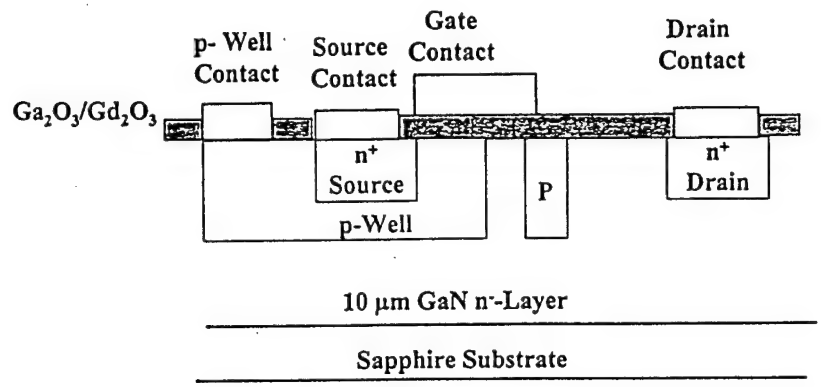

Figure 1. Schematic of an ultra high breakdown voltage GaN power MOSFET.

DRY ETCHING

It is now well-established that high density plasma techniques such as Electron Cyclotron Resonance (ECR) and Inductively Coupled Plasma (ICP) produce much higher etch rates than conventional Reactive Ion Etching (RIE) or low pressure (0.3 mTorr) Reactive Beam Etching (RIBE).

Etching selectivity for one material over another occurs most often when there is formation of an involatile etch product upon exposure of one of the material to the plasma, i.e. presence of a strong chemical reaction. Due to the requirement for a substantial physical component in III-nitride etching due to the strong bonds in these materials, selectivities are generally not that high. In electronic device structures there will be a need to selectively etch InN-based ohmic contact layers from underlying binary or ternary nitride active channel layers.

The issue of sidewall smoothness on laser facets has also received attention recently. Ren et al.[14] reported a number of different methods for minimizing sidewall roughness on dry etched GaN features formed using high density plasmas. In many instances striations on dry etched mesas is a result of roughness in the initial photoresist mask employed, and this roughness is transferred sequentially to the dielectric mask and then to the GaN. Combined with mask erosion during etching, this can produce very smooth sidewalls. Ren et al. reported that flood exposure of the resists, optimization of the bake temperature, choice of plasma chemistry and ion flux/energy for patterning the dielectric mask all influence the final GaN sidewall morphology.

WET ETCHING

Only molten salts such as KOH or NaOH at temperatures above ~250°C have been found to etch GaN at practical rates, and the difficulty of handling these mixtures and the inability to find masks that will hold up to them has limited the application of wet etching in GaN device technology. We have found that AlN and Al-rich alloys can be wet etched in KOH at temperatures of 50-100°C. The Adesida group has recently published several reports on photochemical etching of n-GaN using 365 nm illumination of KOH solutions near room temperature. Rates of 3,000Å·min^{-1} were obtained for light intensities of 50mW/cm^2, and the etch reaction was assumed to be:

$$2GaN + 6h^+ \rightarrow 2Ga^{3+} + N_2 \uparrow$$

The etching was generally diffusion-limited, with somewhat rough surfaces. Intrinsic and p-GaN do not etch under these conditions, and undercut encroachment occurred in some small-scale features due to light scattering and hole diffusion in the GaN itself. This process looks very promising and may be useful for several different fabrication steps in both electronic and photonic devices.

IMPLANT ACTIVATION

Pioneering work by Zolper and Williams et al. has shown that for high implant doses (~5x10^{15}cm^{-2}) amorphous layers will form in GaN at 25°C, and these revert to polycrystalline after annealing up to 800°C, but they do not recover their original crystalline quality even for 1100°C anneals. For lower doses (<10^{14}cm^{-2}), residual damage is detectable by channeling even after 1100°C annealing and this may account for the generally low carrier mobilities observed in implanted material. The use of elevated temperature (200°C) implants did little to reduce accumulated damage. The basic message of this work was that higher annealing temperatures were desirable both the remove the lattice damage and improve the electrical characteristics of the implanted region.

The main problem with use of higher temperature anneals is preservation of the nitride surface. Hong et al. compared use of GaN, InN and AlN powders for providing a nitrogen partial pressure within a graphite susceptor during high temperature rapid thermal annealing. At temperatures above ~750°C, vapor transport of In from InN powder produced In droplet formation on the surface of all nitride samples being annealed. GaN powder was shown to provide better surface protection than AlN powders for temperatures up to ~1050°C when annealing GaN and AlN samples.

Figure 2 shows the rapid annealing times at various temperatures using GaN powder for which surface degradation is first visible by SEM. The areas above each line represent conditions under which there will be clear surface dissociation, whereas the areas below each line represent annealing conditions that will not lead to visible surface degradation. For example, for 10 s anneals under our conditions, any temperature ≥1050°C will lead to pitted GaN surfaces. Changes to the near-surface stoichiometry that affect electrical properties will occur at somewhat lower temperatures than those at which visible surface degradation is obvious (generally by 50-100°C is the rule of thumb for other III-V materials). Therefore the approach of providing

surface protection during annealing by placing powdered nitrides in the reservoir susceptor is not sufficient to prevent some dissociation during implant activation processes in GaN, where temperatures of 1050-1100°C are required. A superior technique is the one reported by Zolper et al. who used sputtered AlN films as encapsulants for annealing implanted GaN at ≥1100°C – the AlN can be selectively removed in KOH solutions after the annealing process. If the data in Figure 2 are replotted in Arrhenius fashion, the slopes (from admittedly a small number of points) yield approximate activation energies of 3.8 eV, 4.4 eV and 3.4 eV, respectively, for GaN, AlN and InN. These are fairly close to the values reported in ref. 24 for dissociation of nitrogen from vacuum-annealed nitrides, i.e. 3.93 eV for GaN, 4.29 eV for AlN and 3.43 eV for InN. Therefore we are confident that the changes in the surface quality for GaN and InN at least are predominantly a result of preferential dissociation of nitrogen during the RTA treatment. For AlN the equilibrium decomposition pressure is much lower than the ambient N_2 pressure in the furnace and at least some of the surface changes in morphology may be due to annealing of crystalline defects.

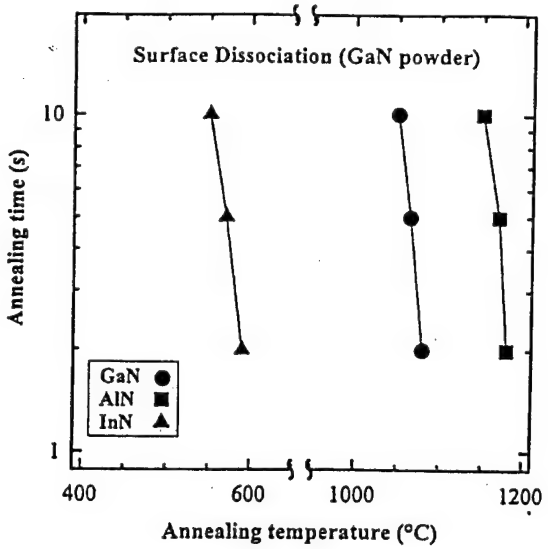

Figure 2. Time-temperature plots for the thermal stability of GaN, AlN and InN surfaces annealed with GaN powder in the susceptor reservoirs. Surface dissociation is visible for annealing conditions to the right of each plot; to the left of each line there is no surface pitting visible by SEM.

While the GaN powder approach works well up to ~1050°C, it clearly does not provide acceptable surface protection for higher temperatures. AlN encapsulant layers can hold up to temperatures of 1400-1500°C, and can be selectively removed by KOH etching at ~80°C after the annealing. Using this approach we have achieved activation efficiencies of ~90% for Si^+ implants (100 keV, $5x10^{15}cm^{-2}$) into GaN, as shown in Figure 3. Note all that the mobilities are above 40 cm^2/Vs for the anneal temperatures of ≥1300°C. The reduction in carrier density at 1500°C may be due to several factors, including Si site-switching and loss of some of the near-surface region through cap failure.

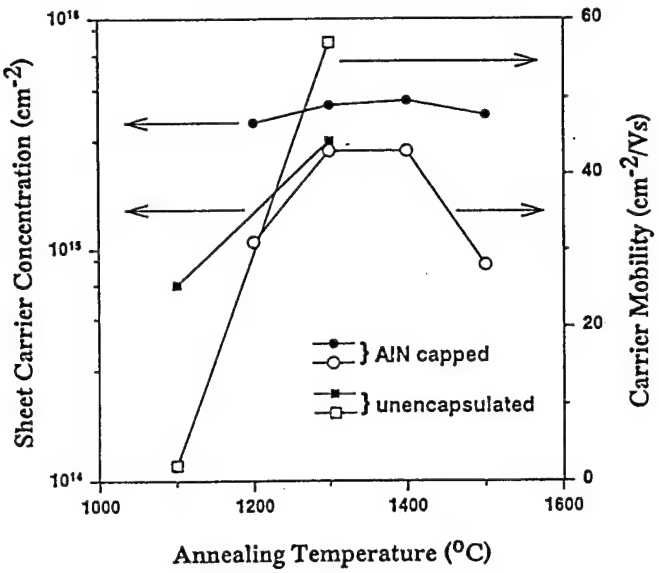

Figure 3. Sheet carrier density and electron mobility in Si^+ implanted (100keV, $5x10^{15}cm^{-2}$) GaN as a function of annealing temperature, either with or without AlN encapsulation. For unencapsulated samples, the GaN is lost by evaporation at ≥1300°C.

IMPLANT ISOLATION

Very effective isolation of AlGaN/GaN heterostructure field effect transistor (HFET) structures has been achieved using a combined P^+/He^+ implant process. The groups of Asbeck and Lau at UCSD demonstrated that a dual energy (75/180 keV) P^+ implant (doses of $5x10^{11}$ and $2x10^{12}cm^{-2}$, respectively), followed by a 75 keV He^+ implant ($6x10^{13}cm^{-2}$) was able to produce sheet resistance of $\sim10^{12}\Omega/\square$ in AlGaN/GaN structures with 1μm thick undoped GaN buffers. The temperature dependence of the resistivity showed an activation energy of 0-71eV, consistent with past measurements of deep states induced in GaN by implant damage.

OHMIC AND SCHOTTKY CONTACTS

There are still large variations in barrier heights reported by different workers for standard metals on GaN. Pt appears to produce the highest consistent values (~1.0-1.1eV) with Ti producing the lowest (0.1-0.6eV). The variability appears to result from the presence of several transport mechanisms, and to materials and process factors such as defects present in these films, the effectiveness of surface cleans prior to metal deposition, local stoichiometry variations, and variations in surface roughness which could affect uniformity of the results. For Schottky contacts P^t appeared to be stable to approximately 400°C for 1h, while PtSi was somewhat more stable (500°C 1h), and also had barrier heights of ~0.8eV.

The commonly accepted ohmic contact to n-GaN is Ti/Al, which is generally annealed to produce oxide reduction on the GaN surface. Multi-level Au/Ni/Al/Ti structures appear to give wider process windows, by reducing oxidation of the Ti layer. R_C values of $\leq 10^{-5}\Omega cm^2$ have been produced on HFET devices using Ti/Al annealed at 900°C for 20 secs.

WSi_X contacts on n^+GaN produce R_C values $\leq 10^{-5}\Omega cm^2$ stable to annealing temperatures of ~1050°C. Reaction with the GaN is relatively limited, although β-W_2N interfacial phases are found after 800°C anneals, and this appears to be a barrier to Ga outdiffusion.

The standard p-ohmic contact to GaN is NiAu, with R_C values $\geq 10^{-2}\Omega cm^2$. Efforts to find a superior alternative has proved fruitless to date, even though strong efforts have been made on multi-component alloyed contacts where one attempts to extract one of the lattice elements, replace it with an acceptor dopant, and simultaneously reduce the "balling-up" of the metallization during this reaction. The model system for this type of contact is AuGeNi/n-GaAs. A promising approach is to reduce the bandgap through use of p-type InGaN on the top of the GaN. To date there have been reports of achieving p-doping ($\sim 10^{17}cm^{-3}$) in compositions up to ~15% In.

GATE DIELECTRICS

Work in this area for power MOSFETs and gate turn-off thyristors is just commencing and some preliminary results are becoming available for AlN, AlON and $Ga(Gd)O_X$, the latter producing excellent characteristics on GaAs and InGaAs and now being applied to GaN. Channel modulation has been demonstrated for AlN and $Ga(Gd)O_X$, but interface, state densities appear well above $10^{11}cm^{-2}$ at this point and much future effort is required to reduce this.

SUMMARY AND CONCLUSIONS

Rapid progress is being made on most of the process modules needed for GaN devices. Apart from the p-ohmic contact on laser diodes and gate dielectrics on emerging power MOSFET and thyristor devices, the processing does not appear to limit the device performance.

AlGaN/GaN '-HEMT's for High Power Microwave Amplifiers

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ABSTRACT

The design and characteristics of AlGaN/GaN piezoelectric HEMT's on sapphire are presented. With .15 μm x 150 μm gates f_t = 67 GHz was measured, and with .15 μm x 75 μm gates f_{max} = 140 GHz was measured. Maximum current was ~ .75 A/mm and extrinsic gm was ~ 200 mS/mm. With 1 μm distance between gate and drain, these devices broke down at 35 V_{ds}. With .33 μm gate length, this breakdown voltage is 70 V_{ds}. The equivalent circuit elements are presented for .28 μm gate length devices, operated at 8 V_{ds} and with ~ .25 A/mm current. Initial power measurement showed up to 75% power-added efficiency at 3 GHz for > 1 W/mm output. Other recent results will be presented.

Introduction

When $Al_xGa_{1-x}N$/GaN is grown on the *c*-face of sapphire, or the equivalent face of semi-insulating SiC, a substantial positive piezoelectric charge develops in the $Al_xGa_{1-x}N$ at the interface. This in turn induces a two-dimensional electron gas (2 DEG) in the GaN with no intentional doping. Such a device has been named a '-HEMT.

For x = 1 the piezoelectric charge magnitude is equivalent to 5 x 10^{13}/cm^2 electrons. Using x = .30 this charge is 1.5 x 10^{13}/cm^2, and the 2 DEG is ~ 1.2 x 10^{13}/cm^2 at V_{gs} = 0, reflecting some gate depletion. The thickness limit of $Al_xGa_{1-x}N$ on GaN is ~ 400 Å to prevent the formation of extra defects. Using Ti/Al/Ti/Au ohmic contacts, annealed at 800° C for one minute, contact resistances ' .5 Ω-mm can be obtained. Using multiple-layer electron beam resist, short Pt/Au mushroom gates can be deposited, yielding high frequency performance. Following S-parameter measurements, the magnitude of the equivalent circuit elements are determined.

Experimental results

The drain current vs. drain voltage, with gate voltage as a parameter, is shown, for a .33 μm gate device in figure 1.

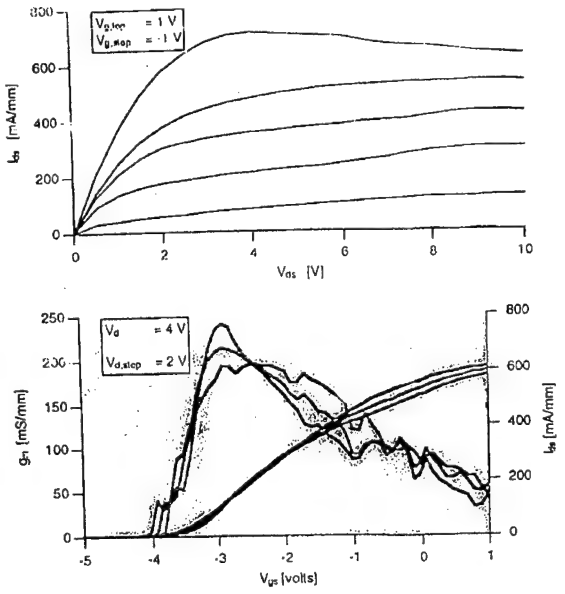

Figure 1

The frequency response of .15 μm gate length devices is shown in figures 2 a (.15 μm x 150 μm) and 2b (.15 μm x 75 μm). The current gain curve with f_t = 67 GHz is for a ' -HEMT with 150 μm periphery, while the power gain

curve with $_{.max}$ = 140 GHz is for ' –HEMT with 75 µm periphery.

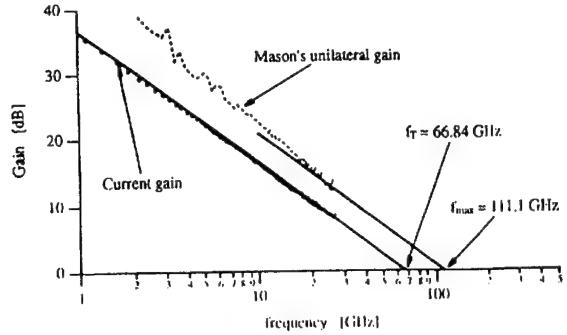

Figure 2 a

These devices had negligible (<< 1 µ A) gate leakage current at pinch–off up to a drain–source break–down of 35 V. The respective $_{.t}$ and $_{.max}$ for devices with .33 µm gate length was 33 · GHz and 111 .GHz, and the drain–source breakdown at pinch–off was 70 V.

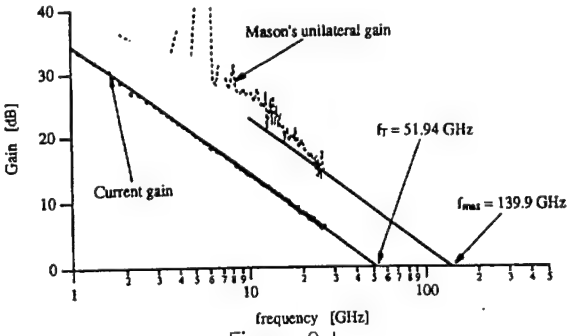

Figure 2 b

Based on the S–parameter measurements, and a standard configuration of circuit elements, the magnitude of some of these elements were determined as listed in Table 1 for a .28 µm gate length device.

Table 1

g_{mi}	257 mS/mm	R_s	1.12 ¼–mm
g_{ds}	13 mS/mm	R_d	1.29 ¼–mm
C_{gs}	.92 pF/mm	C_{gsp}	12 fF
C_{gd}	0.071 pF/mm	C_{gsp}	3 fF
C_{ds}	.085 pF/mm	C_{gsp}	12 fF

Initial power measurements yielded 1–1.5 W/mm, with up to 75% power–added efficiency at 3 GHz.

Discussion

Based on the above results, power amplifiers up to 10–15 GHz with good gain and efficiency are possible using AlGaN/GaN ' –HEMT's. These devices have the expected, well behaved equivalent circuit.

Using the ' –HEMT heat flow simulations of N. Weimann (this workshop), up to 15 W/mm of heat dissipation is possible with parallel gate fingers separated by ³ 30 µm and with SiC substrates. An equivalent amount of microwave power/mm can also be gotten, although ³ 1 A/mm peak current, and ³ 100 V maximum drain current will be required for this much power/mm.

Acknowledgments

The authors are grateful for materials supplied by Dr. K. Boutros of ATMI and Prof. J. Richard Shealy of Cornell University. Initial power measure–ments were made in cooperation with Dr. James Komiak of Lockheed Martin. This research was done with ONR support on MURI contract number N00014–96–1–1223 monitored by Dr. John Zolper.

Technology and Electrical Characterization of AlGaN/GaN HFETs

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[2]Departement of Optoelectronics, University of Ulm, D-89069 Ulm, Germany

DC output I-V characterization and small signal RF performance of AlGaN/GaN FFETs have been investigated. As wide band gap material GaN is predestined for high temperature application. Therefore the FET device was designed for operation at elevated temperatures.

AlGaN/GaN heterostructure field effect transistors were fabricated on a MOVPE grown wafer. The layer-structure includes the sapphire substrate, a 2 μm undoped GaN buffer followed by a 50 nm Si doped GaN channel with a doping density of $5*10^{17}$ cm^{-3} and a 50 nm AlGaN gate layer with an aluminium concentration of 15% (fig.1).

The samples have been cleaned in organic solvent. For electrical isolation of the devices a mesa was realized by dry-etching. For device pattering a double layer resist stack of PMGI and AZ5214E was used for optical gates and a two layer resit stack consisting of PMGI and PMMA for e-beam gates. The ohmic-contact regions were opened by dry etching with a low, controllable etch rate. To reduce the native (Ga) oxide of the free ohmic-contact regions the samples were treated in boiling HCl before metallization. The Ti based with Au overlay ohmic-contact was deposited by ion-beam sputtering annealed at 860°C, 20 sec in N_2. Gate metallization was Pt/Au deposited by electron beam evaporation.

DC output I-V characteristics of AlGaN/GaN FET devices with 1 μm gate and 0.4 μm length were measured. Devices with 0.4 μm gate length and 25 μm gate have an open channel density of 600 mA/mm at 7 V pinch-off voltage (fig.2). From the maximum saturation current and the pinch of voltage a channel doping concentration of $N_D = 8 * 10^{17} cm^{-3}$ and a electron mobility of 300 cm^2/Vs could be extrapolated. Reducing gate length a maximum saturation current of 1 A/mm could be extrapolated for a gate length of 50 nm.

Small signal RF measurements were performed on wafer. For devices with 0.4 μm gate length a $f_t = 10$ GHz and $f_{max} = 20$ GHz at a bias point of 20 V drain-source voltage and -2 V gate-source voltage was obtained (fig.3).

DC device operation has been demonstrated up to 690°C (fig.4).

FIGURES

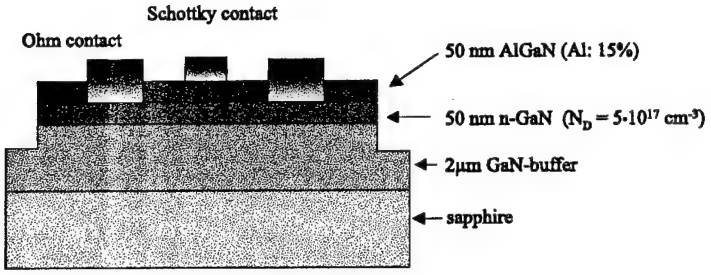

Fig. 1. AlGaN/GaN HFET device structure.

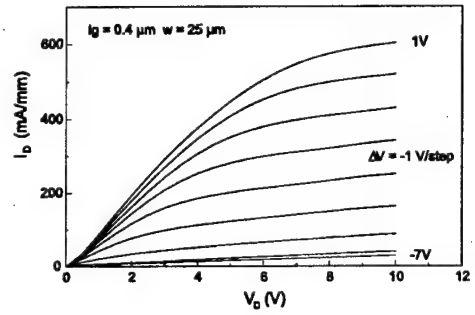

Fig. 2. DC I-V output characteristics at R.T..

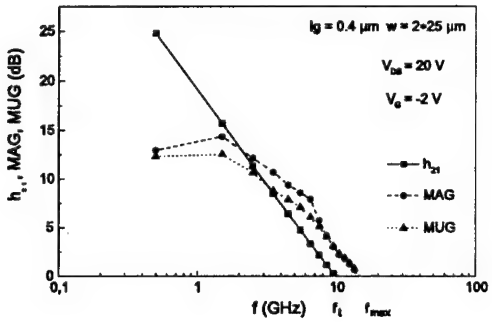

Fig. 3. Small signal RF characteristics.

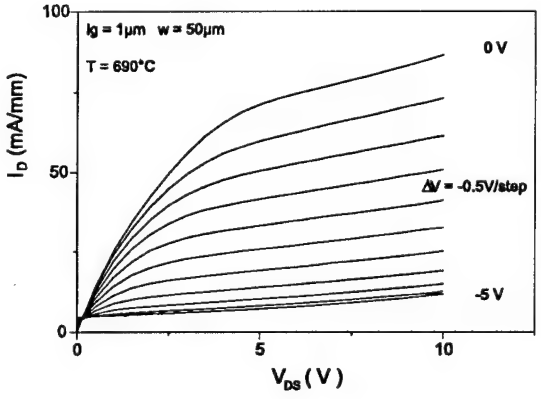

Fig. 4. DC I-V output characteristics at 690°C.

Thermal Simulation of High Power GaN Microwave MODFETs

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The performance of GaN microwave modulation-doped field effect transistors (MODFETs) on SiC substrates may be limited by thermal effects, due to the high power density of these devices. The presented 2D simulation results may be used as guidelines for MODFET design.

The typical layer structure of a GaN MODFET on SiC substrates is depicted in Fig. 1. SiC is used as the substrate material to ensure good thermal conductivity between the active device layer and a heat sink on the backside of the substrate.

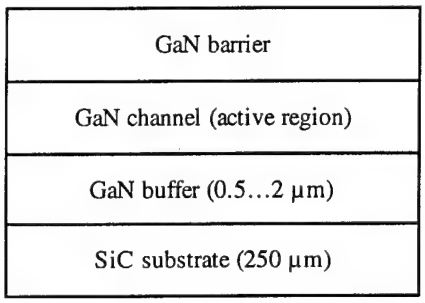

Fig. 1: MODFET epi structure

Heat is generated in the channel between the gate and the drain. The channel is thin (100 Å) compared to the rest of the device structure (250 µm). The heat generation is therefore modeled as a Neumann boundary condition of constant heat flux in the structure over a width of 1.5 µm, which stems from the gate-drain-spacing. The thermal contact on the substrate backside is described by a Dirichlet boundary condition, holding the substrate backside at 300 K. No heat is assumed to flow through the other boundaries. Fig. 2 shows the simulated structure.

For a device consisting of only one gate finger, the simulated region should extend to infinity on both right and left sides. This situation can be approximated assuming a device width which is long compared to the device height, i.e. assuming a width $\geq 500\,\mu m$. The asymptotic behavior of the solution can be seen in Fig. 3.

Geometries involving multiple gate fingers can be modeled by separation into unit cells consisting of one heat source. The width of the unit cell corresponds to the pitch of the device finger layout, given by the distance between gate fingers. The boundary condition of no heat flux through the right and left boundaries is given by the symmetry of the configuration.

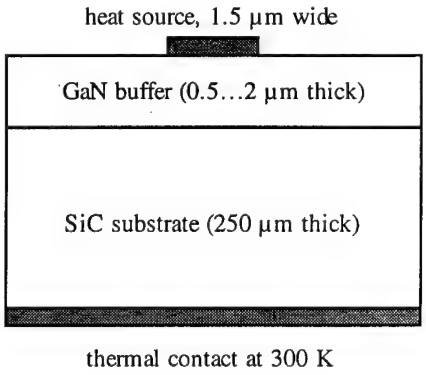

Fig. 2: simulated geometry

The simulation is carried out solving the heat flow equation $-\nabla \cdot k\nabla T = 0$ for the temperature T in two dimensions, using a thermal conductivity k of 1.3 W/cmK in the GaN buffer region, and a thermal conductivity of 5.0 W/cmK in the SiC substrate region. The given thermal conductivities are valid for a temperature of 300 K and assumed to follow a T^{-1} temperature dependence. The now nonlinear partial differential equation problem is solved using a commercial finite element-package (PDE Toolbox for MATLAB™). The mesh typi-

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cally consists of 8000 nodes, with at least 10 points in the heat source boundary segment.

In Fig. 3, the maximum absolute surface temperature is plotted versus gate finger pitch for different GaN buffer thickness. The heat.flow on top of the structure corresponds to a dissipated power of 10 W/mm, scaled to the width of the device.

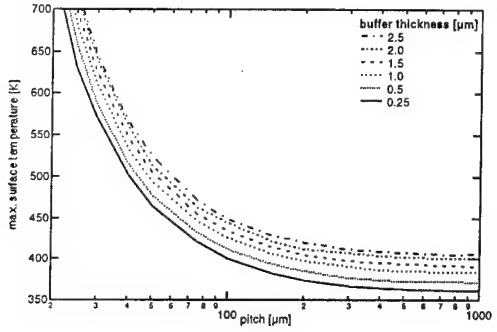

Fig. 3: maximum surface temperature vs. gate finger pitch

For the corresponding heat flux of a given dissipated power, the maximum surface temperature can be converted into an effective thermal resistance $R_{th,eff}$ in units Kmm/W, scaled to the device width in mm, using the relation

$$R_{th,eff} = \frac{T - 300\text{K}}{10\,\text{W/mm}} .$$

plotted in Fig. 4. It is important to include a temperature dependence for the thermal conductivity, simulations assuming a constant thermal conductivity showed an about 20% lower effective thermal resistivity.

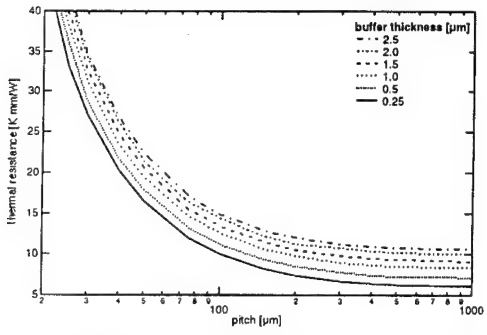

Fig. 4: effective thermal resistance vs. gate finger pitch

By holding the maximum surface temperature at a constant value of 200_C, the corresponding dissipated power is plotted in Fig. 5 versus the gate finger pitch for different GaN buffer thickness.

The thickness of the GaN buffer does not significantly alter the thermal properties of the structure.

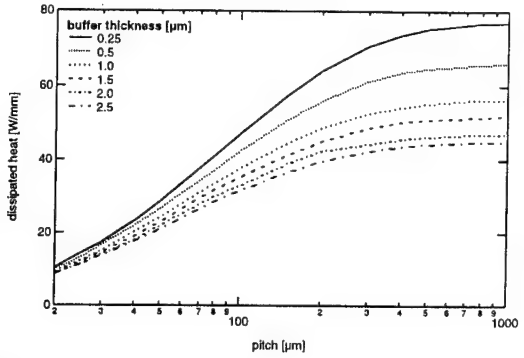

Fig. 5: maximum dissipated power for a max. surface temperature of 200_C

In conclusion, using numerical simulations of heat flow, we have found that the power handling capabilities of the GaN on SiC material system are limited by thermal effects. For a given pitch of 30 µm and a maximum junction temperature of 200°C, the dissipated heat amounts to 15 W/mm. In the case of a sapphire substrate, only 1 W/mm can be dissipated at a pitch of 100 µm, if the channel temperature equals 500 K (see Fig. 6).

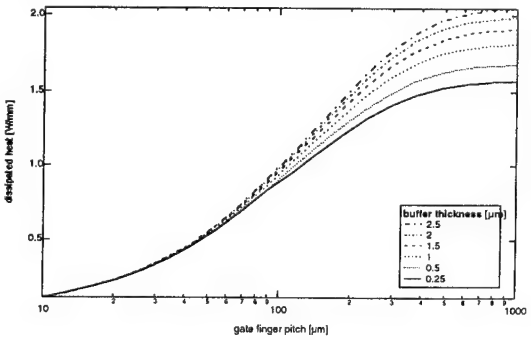

Fig. 6: maximum dissipated power on a sapphire substrate, channel at 200_C

Research is supported by the ONR under MURI contract no. N00014-96-1-1223, monitored by Dr. John Zolper.

Session 10: Novel Devices

9: 00 **Semiconductor Heterostructures: A Quantum LEGO™ for the Infrared Technology**
E. Rosencher — *invited*
Thomson-CSF, Orsay — France

9: 30 **Simulation and Robustness Evaluation of a Quantum Cellular Automata Basic Cell**
M. Governale, *M. Macucci,* G. Iannaccone, C. Ungarelli
Università di Pisa — Italy

9: 40 **Admittance Engineering for RTD's and HBV's**
O. Dupuis, X. Melique, P. Mounaix, F. Mollot, O. Vanbèsien, D. Lippens
UMR CNRS, Villeneuve — France

9: 50 **Manufacturability and Prospects of RTD/HFETs for Digital Circuitry of Reduced Complexity on InP**
W. Prost, C. Pacha, U. Auer, A. Brennemann, K. F. Goser, F.-J. Tegude
Gerhard-Mercator-Universität, GH Duisburg — Germany

10: 00 **Combination of SAW and Semiconductor Heterostructures: A New Class of Devices**
M. Streibl, M. Rotter, C. Rocke, A. Wixforth
LMU, Sektion Physik, München — Germany

10: 10 **Monolithic Tandem Solar Cell Based on AlGaAs/Si System**
L. Semra, *M. Remram*
Universitè de Constantine, Constantine — Algeria

10: 20 **A Matched InGaAs Detector Diode for a Ka-Band Radar Front-End**
C.G. Diskus, A. Stelzer, K. Lübke, A. L. Springer, G. Haider, H. W. Thim
Johannes Kepler University, Linz — Austria

SEMICONDUCTOR HETEROSTRUCTURES: A QUANTUM LEGO™ FOR THE INFRARED TECHNOLOGY

Emmanuel ROSENCHER
Laboratoire Central de Recherches de THOMSON-CSF
ORSAY

Growth technologies allow different semiconductor layers to be epitaxially grown on top of each other with a one atomic monolayer precision. In such structures, motion of electron and holes are quantized in the growth direction, forming quantum wells whose thickness, depth and more generally any shape can be tailored to engineer and optimize specified functions based on quantum phenomena such as photoemission, optical non linearities, stimulated emission,...In the same way, photons may also be confined in complex optical index engineered heterostructures in which new optical nonlinearity effects are obtained. These devices have dramatically changed the field of infrared technology industry. In this Communication, we will address more specifically the realizations in the following fields:

- Quantum Well Infrared Photodetectors arrays for high definition infrared imaging and quantum engineered new functions such as tunability, multispectrality,...
- Optical frequency convertors stressing the properties of GaAs/AlOx heterostructures for all solid state optical parametric oscillators (OPO) applications
- Unipolar and Bipolar Quantum Cascade lasers

SIMULATION AND ROBUSTNESS EVALUATION OF A QUANTUM CELLULAR AUTOMATA BASIC CELL

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During the last few years, several ideas for the implementation of logic functions and data processing based on the Quantum Cellular Automata concept and "ground state computation" have been presented. The architecture commonly known as "Notre Dame architecture" is based on bistable cells which couple electrostatically to the nearest neighbors. Each cell is made up of four (or five) quantum dots containing two electrons, which, in the absence of external electric fields and if the potential barriers defining the dots are large enough as to strongly localize their wave functions, will align with equal probability along one of the two diagonals. In the presence of a nearby cell polarized in one of the two possible bias conditions (driver cell), the alignment along the diagonal parallel to that occupied in the driver cell will be energetically favored in the driven cell. On the basis of this principle, it is possible to conceive two-dimensional layouts of bistable cells, in which the polarization state enforced at the inputs propagates across the array, until the ground state is reached throughout the system, and the results of the computation can be read in the form of the polarization state of the output cells.

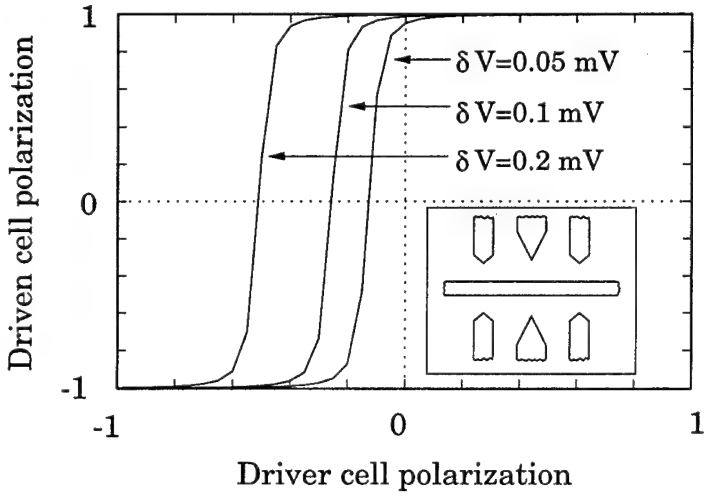
The main purpose of the work we are presenting is to investigate the basic building block for this architecture, made up of two coupled cells, defined by means of metal gates, depleting the two-dimensional electron gas obtained at a GaAs/AlGaAs heterointerface. We have been interested in establishing the robustness of cell-to-cell operation to asymmetries in the gate geometries or in the bias voltages.

The model we have used in our computations consists of four quantum dots defined by realistic two-dimensional potentials, evaluated from the shape of the metal gates at the surface of the heterostructure and the voltages applied to them, with the addition of the electrostatic interaction from the nearby driver cell.

Calculation of the electron density in such a 2-D artificial molecule is a challenging task: iterative self-consistent methods fail to converge, due to the strong electrostatic interaction and to the particular symmetries associated with the problem. To overcome these convergence problems we have developed a non-iterative technique based on the Configuration-Interaction method used in molecular chemistry.

We have first analyzed the dependence of the cell-to-cell response function, defined as the polarization of the driven cell versus that of the driver cell, on geometrical asymmetries, varying the size or the position of one of the gates defining it. Since the energy splitting between the two configurations is extremely small, very limited size perturbations and the ensuing variations of the confinement energy are sufficient to disrupt the operation of a cell.

Then, we have investigated the effects of asymmetries in the gate voltages, evaluating the dependence of the cell-to-cell response function on small, asymmetric perturbations of the gate voltages. In the figure below we show the results obtained for a driven cell defined by seven gates (the layout is represented in the inset), in a 2DEG at a depth of 50 nm from the semiconductor surface, when the voltage applied to the upper right gate is varied by an amount δV.



From the results of the robustness analysis, design criteria for quantum cellular automata cells are derived, and their practical implementation is discussed.

22nd Workshop on Compounds Semiconductor Devices and Integrated Circuits, May 24-27, 1998

ADMITTANCE ENGINEERING FOR RTD'S AND HBV'S

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In this communication, we report on the design and the characterization of high performance Resonant Tunneling Diodes (RTD's) and Heterostructure Barrier Varactors (HBV's) aimed at operating at millimeter and submillimeter wave-lengths. The originality of the structures stems from the systematic use of strained layers which permits us to combine quantum confinement and tunneling effects for enhancing the non linearity of the devices. Potential applications concern the harmonic multiplier chains and solid sources at terahertz frequencies. In the present work, particular emphasis was paid to the InP-based material system but the design rules through potential perturbations can also be adapted to the GaAs material system as demonstrated by our team and by the MIT high speed device group [1]-[2].

For the resonant tunneling devices, the main idea was to introduce a potential perturbation by means of an InAs quantum layer as depicted in inset of Figure 1. This scheme was already used successfully over the past and was employed in this work for the fabrication of very high current density devices while preserving the peak-to-valley current ratio for a room temperature operation. In Figure 1, we show the current-voltage characteristic calculated by means of a home-made self-consistent Poisson-Schrödinger equations solver applied to the structural parameters of Figure 2a. Figure 3 shows the corresponding experimental data. For the devices under test, the peak current density is as high as 210 kA/cm^2 for peak-to-valley current ratios between 3:1 and 5:1 which compare favorably to the best results achieved so far in the InP material system.

With respect to the HBV's technology, the novelty of the design comes from the use of pre-well and post-well layers grown prior and after the growth of the single barrier blocking layer (Figure 2b). The key advantage afforded by this quantum-well / blocking barrier configuration is that the capacitance modulation results from the variation of the sheet carrier density trapped in the well rather than the conventional depleted zone edge modulation. Under these conditions, much better performance in terms of nonlinear capacitance can be expected. The demonstration of the validity of this concept was made by means of InGaAs/InAs/InAlAs/AlAs layers with a pseudomorphic growth on an InP Substrate. The C(V) curve measured at 500 MHz is reported in Figure 4 . The performances were beyond our hopes with a capacitance ratio C_0/C_{sat} deduced from values at equilibrium and before breakdown as high as 7:1 for a voltage handling of about 8 V.

To assess the frequency capability of the present devices, we summarize in Table 1 their key figures of merit along with the relevant cut-off frequencies. The series resistance values were measured from small signal impedance measurements of devices integrated with coplanar footprints for wafer probing. For both types of devices it is found that the spreading resistance is the major contribution to the overall series resistance and hence does not scale with area. The diode area was chosen on the basis of power capability and impedance matching to the circuit considerations. The cut-off frequencies for RTD's and HBV's are about 200 GHz and 2 THz respectively and could be further increased through the use of shrunk lateral dimensions.

[1] R. Bouregba et al.,' Resonant tunneling diodes as sources for millimeter and submillimeter wavelengths', IEEE trans. Microwave Theory and Techniques Vo. 41, pp. 2025, 1993

[2] C. L. Chen,' New Self-aligned planar resonant diodes for monolithic circuits', IEEE Electron Dev. Lett. Vol. 18, Pp; 489, 1997

[3] E. Lheurette et al., 'Capacitance engineering for InP-based Heterostructure Barrier Varactor , submitted to publication

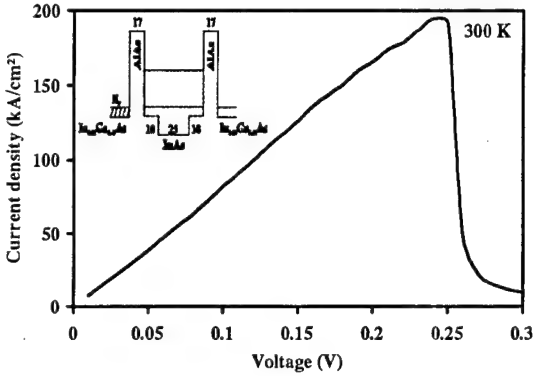

Figure 1 : Current-voltage characteristic calculated

Contact layer	$In_{0.53}Ga_{0.47}As$	>1x10^{19} at.cm-3	5000 Å
Cladding layer	$In_{0.53}Ga_{0.47}As$	1x10^{18} at.cm-3	1000 Å
Spacer	$In_{0.53}Ga_{0.47}As$	n.i.d	50 Å
Barrier	AlAs	n.i.d	17Å
Well	$In_{0.53}Ga_{0.47}As$	n.i.d	10 Å
	InAs	n.i.d	25 Å
	$In_{0.53}Ga_{0.47}As$	n.i.d	10 Å
Barrier	AlAs	n.i.d	17 Å
Spacer	$In_{0.53}Ga_{0.47}As$	n.i.d	50 Å
Cladding layer	$In_{0.53}Ga_{0.47}As$	1x10^{18} at.cm-3	1000 Å
Contact layer	$In_{0.53}Ga_{0.47}As$	>1x10^{19} at.cm-3	5000 Å
Buried layer	InP	5x10^{18} at.cm-3	5000 Å

Fe-doped Semi-Insulating InP substrate

(a)

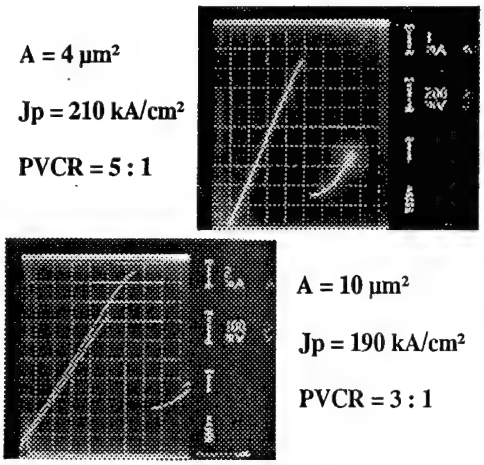

Figure 3 : I-V characteristics measured at 300 K (b)

Contact layer	$In_{0.53}Ga_{0.47}As$	5x10^{18} at.cm-3	3000 Å
Cladding layer	$In_{0.53}Ga_{0.47}As$	1x10^{17} at.cm-3	3000 Å
Pre-well	InAs	n.i.d	50 Å
Spacer	$In_{0.53}Ga_{0.47}As$	n.i.d	10Å
Blocking barrier	InAlAs	n.i.d	50 Å
	AlAs	n.i.d	30 Å
	InAlAs	n.i.d	50 Å
Spacer	$In_{0.53}Ga_{0.47}As$	n.i.d	10 Å
Post-well	InAs	n.i.d	50 Å
Cladding layer	$In_{0.53}Ga_{0.47}As$	1x10^{17} at.cm-3	3000 Å
Contact layer	$In_{0.53}Ga_{0.47}As$	5x10^{18} at.cm-3	5000 Å
Buried layer	InP	5x10^{18} at.cm-3	10000 Å

Fe-doped Semi-Insulating InP substrate

(b)

Figure 2 : Structural parameters of RTD's (a) and HBV's

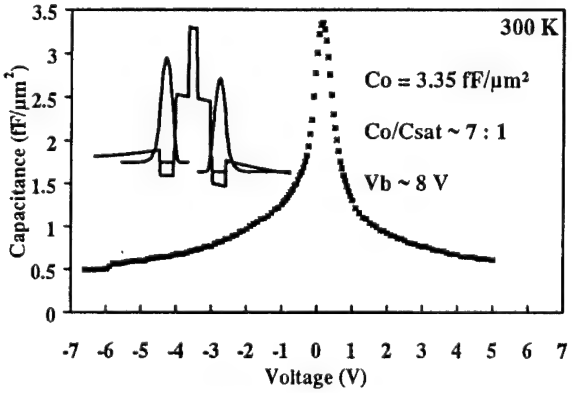

Figure 4 : Capacitance-voltage characteristic for a pre-well/post-well HBV

TYPE	Cd	Rd	Rs	Fc
RTD's (10 µm²)	Co = 67 fF	22.5 Ω	5 Ω	197 GHz
HBV's (60 µm²)	Csat = 29.7 fF Co = 201 fF	40 kΩ V < 8 V	2.5 Ω	1.85 THz

Table 1 : Key figures of merit for the devices under test along with their relevant cut-off frequencies

submitted to WOCSDICE;
Zeuthen Germany, May 24-27, 1998

MANUFACTURABILITY AND PROSPECTS OF RTD/HFETS FOR DIGITAL CIRCUITRY OF REDUCED COMPLEXITY ON INP

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ABSTRACT: The progress in digital circuits primarily resulted from the scaling of Silicon-based transistors. From the SIA roadmaps, it is expected that this strategy will sustain in the next decade even if the channel length of industrial fabricated transistors declines 100 nm with according oxide thickness of less than 5 nm. The final goal is the realisation of electronic switching with a tremendously reduced number of electrons e.g. in a Single Electron Transistor (SET). In order to allow SET operation at room-temperature a feature size in the order of one nanometer is required. In addition, due to the off-set charge problem, the reduction of the electron number per operation is limited and especially the realisation of logic circuitry is very unlikely within the next decade.

One alternative is the development of circuits with higher computational functionality. This alternative currently motivates strong efforts on this subject using resonant tunnelling devices (RTD) combined with three-terminal transistors [1,2]. In this contribution, we report on the realisation of RTD/E-HFET on InP as building blocks for digital circuitry following the approach given in [1] and we will stress the applicability of this building block in a novel circuit architecture (multiple input threshold logic). For this purpose, the design of low-peak voltage RTD and enhancement-type HFET will be presented and a preliminary investigation on manufacturability will be given. Various III/V-layer structures were grown by MBE and small area DB-RTD were processed. The homogeneity and reproducibility of the layers will be presented and correlated with I-V-characteristics. Finally, the reduction of circuit complexity will be predicted for a full adder building block.

Using MBE, an InP-based DB-RTD is developed for digital applications. A low peak voltage and a low peak current is adjusted due to thin barriers (8 ML InAlAs) and thick wells (InGaAs/InAs/InGaAs 4/8/4 ML). A self-aligned small area device technology has been developed allowing an accurate and reproducible device area definition. A study on three nominally identical runs (cf. Table 1) revealed a peak voltage and peak current homogeneity of better than 2.7 % and 5.1 %, respectively, while the reproducibility was within 9.4 % and 6.9 %, respectively. We will show that the aspect of layer data was overestimated in the past, especially if the device dimensions are shrinking according to low-power digital circuit applications [2].

In Fig. 1 an inverter as basic building block of a dynamic logic family is shown. Two series connected RTDs operate as a bistable switching element as proposed by Chen et al. [1]. The FET T1 causes a small peak current modulation in the bottom switching RTD. At the rising edge of the clock voltage this current modulation forces the output into a stable state above (T1 off) or below the peak voltage (T1 on). In order to switch a following gate the output voltage has to be lower than the threshold for the off-state or below the maximum allowed bias voltage for the

Sample	V 101	V 102	V 103	unit
yield	17/17	16/17	19/19	
V_{Peak}	286	232	226	mV
$\pm \sigma V_{Peak}$	5	5	6	mV
I_{Peak}	5.64	5.4	4.66	kA/cm²
$\pm \sigma I_{Peak}$	0.13	0.56	0.24	kA/cm²

Tab.1: Yield and I-V-data (mean value, standard deviation) of 3 nominally identical InP-based DB-RTD (A_E=30 μm²)

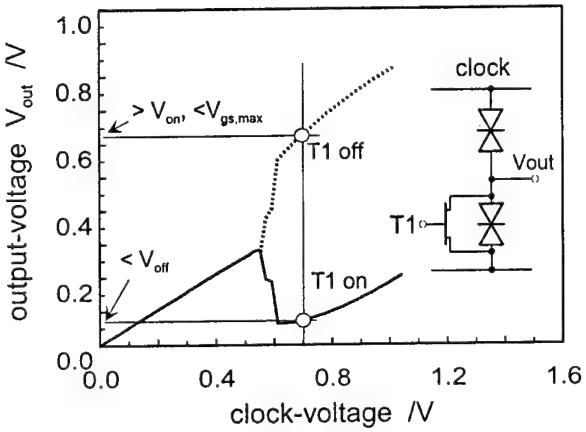

Fig. 1: Basic switching block composed of two series connected RTD with a parallel FETs for forcing the upper or the lower RTD above the peak voltage

on-state. Accordingly, an Enhancement-type HFET (E-HFET) is urgently required because depletion-type FET would increase the complexity of circuit and are not allowed if low complexity circuits are intended. E-HFETs on InP are a critical issue because of the low Schottky barriers available in this material system. Characteristics of E-HFETs fabricated and monolithically integrated with RTDs of the above described type are depicted in fig. 2. Transistors with a threshold of +0.1 V are operated up to a gate bias of 1 V. In Fig. 1 the output characteristics and the gate leakage is given. For digital applications an E-HFETs with low current density and a gate length of 1 µm exhibit a transconductance of 240 mS/mm. For the intended maximum gate bias of 0.6 V the gate leakage is below 2 mA/mm and hence suitable for logic circuitry.

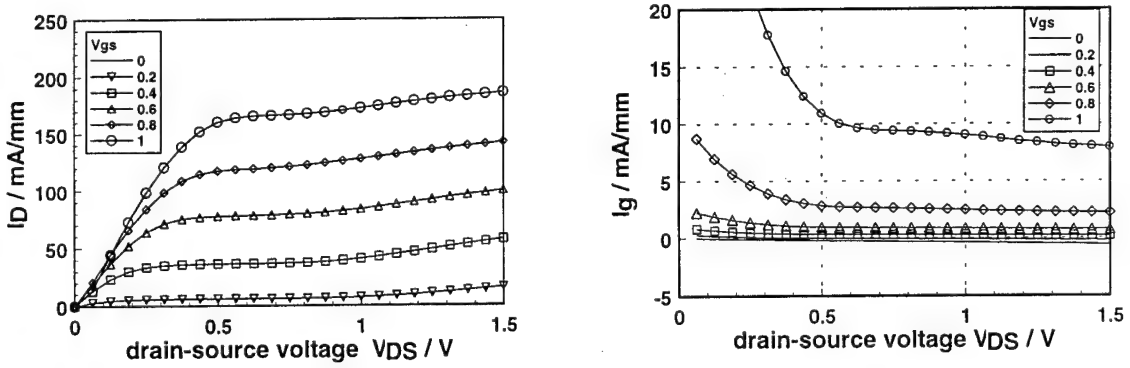

Fig. 2: I-V-characteristics of an InP-based E-FET (Wg = 30 µm, Lg = 1 µm)

Based on the RTD/HFET modules a threshold logic gate is aimed at, where the single FET T1 is substituted by multiple, parallel FETs to implement the multiple inputs. The principal expected result is to verify experimentally the predicted reduction of the complexity for threshold logic circuit components. The starting point of this verification are the theoretical predictions of S. Vassiliadis and his group [3]. In the case of an full adder building block the threshold logic version reduces the logic depth, that is the number of subsequent circuit layers from 6 (static CMOS NAND/NOR family) to the minimum logic depth of 2. This advantage on the level of small LTG circuits will lead to an estimated reduction of the logic depth of about 50% on the module level (n-bit adder). If more advanced circuit components including bit-level pipelining and specially adapted parallel computing schemes are used a performance gain of more than one order of magnitude is achievable for 64 bit operands compared with a boolean implementation.

Literature:

[1] K. Chen, K. Meazawa, M. Yamamoto: InP Based High Performance Monostable-Bistable Transition Logic Elements (MOBILE's) Using Integrated Multiple-Input Resonant-Tunnelling Devices, IEEE Electron Device Letters, Vol. 17, No. 3, March 1996, pp. 127-129.

[2] L. Chen, R.H. Mathews, L.J. Mahoney, P.A. Maki, K.M. Molvar, J.P. Sage, G.L. Fitch, and T.C.L.G. Sollner: New Self-Aligned Planar Resonant-Tunnelling Diodes for Monolithic Circuits, IEEE Electron Device Letters, Vol. 18, No. 10, pp. 489-491, 1997.

[3] S. Cotofana, S. Vassiliadis, Low Weight and Fan-In Neural Network for Basic Arithmetic Operations, Proceedings of the 15th IMACS World Congress on Scientific Computation, Modelling and Applied Mathematics, Vol. 4, Berlin, August 1997, pp. 227-232.

Combination of SAW and semiconductor heterostructures: A new class of devices

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The combination of surface acoustic waves (SAWs) and the superior electrical and optical properties of band gap engineered semiconductor layer systems yields a completely new and promising approach toward another generation of acoustoelectric and optoelectronic devices.
SAWs are modes of elastic energy that propagate on the surface of a crystal at the speed of sound. If the solid is piezoelectric, which most of the III-V materials like AlGaAs and InGaAsP systems are, these waves not only generate a dynamic stress field within the semiconductor but are accompanied by strong electric fields and potentials.
The deformation and the travelling electric potential modulation can be exploited to alter the electrical and optical properties of a semiconductor sample over a wide range [1].
In direct gap semiconductors, incident light is efficiently converted into loosely bound electron-hole pairs (excitons), which usually live for mere nanoseconds before recombining in a flash of light with a characteristic energy distribution (Photoluminescence/PL).
The strong lateral piezoelectric fields accompanying a SAW can now break these excitons apart before their radiative decay. The remaining fragments (free electrons and holes) are then collected in the travelling potential minima of the acoustic wave.
Since electrons and holes find their energetic minimum half a wavelength (about a micron) apart, the overlapp between their wavefunctions is neglectible and the recombination is delayed as long as they are confined within the SAW fields.
These free carriers, "surfing" in the potential ripples of the SAW can then be used to realise a totally new set of optoelectronic applications in signal processing and optical computing.
Our basic device [2] [3] could be called a "conveyor belt" for photons. As described above, a light pulse coupled onto the SAW-beam will convert itself into pairs of surfing electrons and holes. As soon as the carriers reach a sort of artificial "beach", i.e. an area within the device where the SAW-potential is in some way supressed, electrons and holes will find each other and reconvert themselves into a lightpulse.
Thus, this device fulfills two tasks: it delays a light signal by the travelling time of the SAW (microseconds) and simultaneously transports the transformed light pulse to a sample area where additional signal processing can take place.
Furthermore, it would be possible to pump an optical active area with these travelling carriers, a mechanism which could be summarized as acoustic carrier injection. It should be emphasized that this acoustic injection mechanism has an built-in internal clock which ticks at the SAW frequency. In combination with low dimensional electron systems it can be used to realize a novel quantum-optic device, a "light source" with absolute strict time correlation between emitted photons.
A SAW not only modulates the optical properties of a semiconductor structure by its piezoelectric fields and the resulting dynamic bandgap, but also by the influence of the huge accompanying stress fields which modulate the refractive index n of the material. The interest is focused here on the realisation of tunable dynamic bragg reflectors and waveguide structures. Acousto-optical modulators based on passive materials like $LiNbO_3$ are well established on the optoelectronics market. The integration of SAW-driven modulators with optical active semiconductor structures like lasers and photodiodes, however, is still of great interest.
Finally, to focus on acoustoelectric applications, it is the combination of the excellent electronic

properties of a semiconductor heterojunction and the acoustic properties of a strong piezoelectric material like $LiNbO_3$ that yields very promising SAW hybrid devices. Quasi-monolithical integration of MBE grown semiconductor quantum well structure on a $LiNbO_3$ SAW device is achieved using the epitaxial lift-off (ELO) technique. The active semiconductor layer system is removed from its substrate and transfered onto the $LiNbO_3$. The conductivity of the two-dimensional electron system in the quantum well, which can be controlled via field-effect, modifies the velocity of the surface acoustic wave. The electromechanical coupling coefficient of $LiNbO_3$ is nearly a factor 100 higher than for bulk GaAs. Thus the coupling between SAW and electron system is strongly enhanced and results in a large phase shift of the travelling wave. As an example for a new class of voltage-tunable single chip SAW devices a voltage-controlled oscillator (VCO) [4] [5] is presented, in which the output frequency can be tuned by an applied gate voltage.

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[1] A. Wixforth, J. Scriba, M. Wassermeier, J.P. Kotthaus, G. Weimann und W. Schlapp, *Phys. Rev. B* **40**, 7874 (1989)

[2] C. Rocke, S. Zimmermann, A. Wixforth, and J. P. Kotthaus, Phys. Rev. Lett. **78**, 4099 (1997).

[3] *American Institute of Physics*, http://www.aip.org/physnews/graphics, "Photon conveyor belt".

[4] M. Rotter, A. Wixforth and J. P. Kotthaus, IEEE Ultrasonics Symposium 1997 in Toronto, Canada.

[5] M. Rotter, C. Rocke, S. Böhm, A. Lorke, A. Wixforth, W. Ruile, L. Korte, Appl. Phys. Lett. **70** (16), 2097 (1997).

MONOLITHIC TANDEM SOLAR CELL BASED ON AlGaAs/Si SYSTEM

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Abstract: High efficiency photovoltaic devices are based both on the III-V compounds and silicon semiconductor technologies. These devices are of both single and multijunction configurations. A tandem solar cell including more than two junctions is one of the candidates for photovoltaic cell. Among many material systems, the AlGaAs/Si monolithic tandem solar cell is attractive for its high efficiency, low cost and large-area photovoltaic cell from the band-gap-energy point of view.

The aim of this work is focused on semiconducting materials in Si and $Al_xGa_{1-x}As$ on the Si substrate and the AlGaAs/Si monolithic tandem solar cell. The optimum efficiency is determined taking into account the different factors affecting the photogenerated current, open circuit voltage and fill factor.The most considerable subject of this study in the top cell is its emitter region. The judicious choice of aluminium content of the AlGaAs layer is the particular considered point, because results reveal that efficiency decreases with increasing Al composition. This is due to the increase of the bandgap which lower the absorption coefficient and to the fact that minority carrier lifetime is degraded with the increase of Al composition. Also the thickness and doping concentration are examined. Shallow and highly doped emitter improve the efficiency. High doping level effects in Si solar cells (the bottom cell) in the two regions particularly in the base are investigated taking into account the free carrier absorption. these improve considerably the open voltage and efficiency. Since, the AlGaAs/Si tandem solar cells are promising for both terrestrial and space applications, it is the object of this work to perform modeling studies in one dimension and to determine their reachebel global maximum and AM0 efficiencies. A GaAs layer is introduced between the top cell and the bottom one in order to reduce dislocations therefore the high recombination velocities at the heteroface, due to the lattice mismatch and the difference in the thermal expansion coefficient, and improve efficiency. Modeling and simulation are performed using PC1D simulator. Results are compared with those obtained from other studies.

A Matched InGaAs Detector Diode for a Ka-Band Radar Front-End

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Abstract— *Experimental results with a 35 GHz Doppler radar unit are reported in this contribution. The measurement setup consists of a RF-front-end, signal conditioning, signal processing and a display unit. The sensitivity of the receiving part has been enhanced by matching a recently developed InGaAs-detector diode with the characteristic impedance of the microstrip transmission line.*

RF-Unit

Transmitter

In order to minimize costs a special planar Gunn-diode (FECTED, Field Effect Controlled Transferred Electron Device) has been used instead of a sophisticated transistor oscillator [1]. The output power of the oscillator is fed into a transmitting antenna.

Receiver

At the mixer diode the reflected signal from a receiving antenna is combined with the LO signal provided by a 10 dB directional coupler. To achieve mixing with high sensitivity at zero bias an InGaAs-Schottky-diode has been developed.

Antennas

A relatively inexpensive RT/duroid® 5880 (a trademark of Rogers Corp.) substrate material has been used for the fabrication of the antennas and the 10 dB directional coupler. Each antenna consists of 8x8 microstrip patches yielding a beamwidth of 8 degrees [2].

Matched $In_{0.38}Ga_{0.62}As$-Schottky Detector Diode

The voltage sensitivity of a detector diode is a function of the reverse saturation current. For optimum sensitivity this current has to be in the range of 10^{-6} A. To achieve this value with GaAs technology at zero bias – which is desirable to keep the circuit as simple as possible – the barrier height must be tailored to 0.22–0.25 eV by incorporating Indium. The characteristics of such a diode with an In content of 38% has been reported in [3].

For reduced bandwidths the sensitivity of 1 mV/µW can be further improved by matching the impedance of the diode to the characteristic impedance of the transmission line. The equivalent circuit of the diode has been deduced from network analyzer measurements and is depicted in Fig. 1. For the frequency range of 34–36 GHz a matching circuit consisting of a microstrip stub terminated by a radial stub has been designed. The resulting reflection factor is shown in Fig.2. With this design a sensitivity of 6 mV/µW has been obtained.

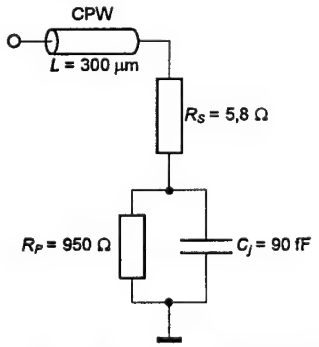

Fig. 1: Equivalent Circuit of Detector Diode

Signal Conditioning and Signal Processing

To guarantee a sufficiently high signal level at the A/D-converter an amplifier with automatic gain control (AGC) is provided. A band-pass filter enhances the quality of the signal by eliminating both noise and low frequency variations. The Doppler-signal ist converted with a resolution of 16 bit. The signal processing is performed on a DSP-board (Digital Signal Processor) equipped with a SHARC (Super Harvard Architecture Computer, Analog Devices Inc.) signal processor. The DSP separates the signal from noise and spurious responses and determines the actual frequency of the Doppler-signal which is proportional to the target velocity.

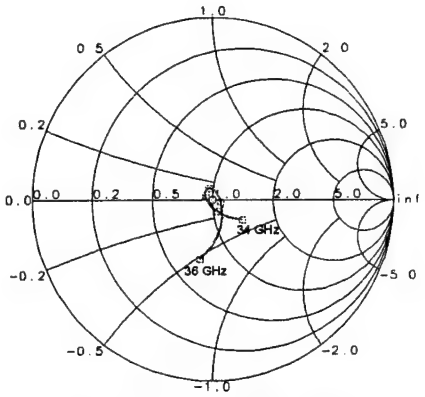

Fig. 2: S_{11} of Matched InGaAs-Detector Diode

Technical Data

Oscillator	
Type:	FECTED
Frequency:	35 GHz
Tuning Range:	350 MHz
Tuning Sensitivity:	0.6 MHz/mV
Output Power:	10 dBm
Phase Noise:	–90 dBc/Hz @ 1 MHz off carrier
Detector	
Type:	Schottky
Material:	$In_{0.38}Ga_{0.62}As$
Area:	3 x 3 μm^2
Matching (50 Ω):	Microstrip T-Structure, 35 GHz
Sensitivity:	6 mV/μW

Antenna:	
Type:	Linearly Polarized Microstrip Patch Array Antenna
No. of Elements:	8 x 8 = 64
Substrate:	RT/duroid® 5880, $\varepsilon_r = 2.2$
Power Gain:	22 dB (Isotropic)
Beamwidth:	± 5° (–3 dB)
Data Aquisition:	
AGC-Amplifier:	20–75 dB
Bandwidth:	10 Hz–3.3 kHz
A/D-Converter:	16 bit, max.100 kHz
DSP:	Analog Device ADSP-2106x, SHARC, 120 MFLOPS
Algorithms:	Filtering, FFT, Averaging

Results and Outlook

The speed sensor has been built and evaluated using an automatic test bench. An accuracy of 0.1% has been achieved in the case of a corner reflector moving at constant speed. The maximum operational range exceeds 25 m. The amplitude of the output signal of the mixer was 0.3 mV_{pp} at this distance.

References

[1] C. G. Diskus, K. Lübke, A. L. Springer, H. W. Lettenmayr, H. W. Thim: "GaAs Field Effect Controlled Transferred Electron (FECTED) Oscillator MMIC", WOCSDICE '92

[2] A. A. Efanov, H. W. Thim, "Corporate-Fed 2x2 Planar Microstrip Patch Sub-Array for the 35 GHz Band", *IEEE Antennas and Propagation Magazine*, vol. 37, no. 5, pp. 49–51, Oct. 1995

[3] K. Lübke, T. Hilgarth, C. Diskus, A. Stelzer, A. Springer, H. W. Thim: "Zero-bias Detection with $In_{0.38}Ga_{0.62}As$ Schottky Barrier Diodes", WOCSDICE '97, pp. 114–115

Session 11: Simulation and Noise Characterization

11: 00 **Large Signal Modelling Through EM and HB Simulations**
J. Carbonell, R. Havart, P. Mounaix, O. Vanbèsien, J. M. Goutoule
D. Lippens
UMR CNRS, Villeneuve — France

11: 10 **A Nonlinear, Scaleable FET Model Including Temperature Dependence and Noise Effects**
R. Follmann, J. Herrmann, R. Tempel, I. Wolff,
IMST, Kamp-Lintfort — Germany

11: 20 **SiGe HBT in Mixed-Mode Device and Circuit Simulation**
V. Palankovski, T. Grasswer, S. Selberherr
TU Vienna — Austria

11: 30 **A New Experimental Technique for Phonon Engineering: Characterization on InGaAs-Based 2 DEG Channels**
A. Matulionis, A. Aninkevicius, J. Berntgen, H. L. Hartnagel, K. Heime,
J. Liberis
Semiconductor Physics Institute, Vilnius — Lithuania

11: 40 **2 D Electron Subband Population and Mobility in a GaAs Quantum Well With a Thin AlGaAs Barrier**
J. Pozela, K. Pozela, V. Juciene, A. Namajunas
Semiconductor Physics Institute, Vilnius — Lithuania

11: 50 **Low-Frequency Noise Studies in AlGaN/GaN HEMT's**
J. A. Garrido, F. Calle, I. Izpura, E. Munoz, J. L. Sanchez-Rojas,
R. Li, K. L. Wang
Ciudad Universitaria, Madrid — Spain

12: 00 **Mobility Dependence of the Low Frequency Noise of 2DEG structures**
J. Berntgen, A. Matulionis, K. Heime
RWTH Aachen — Germany

22nd Workshop on Compounds Semiconductor Devices and Integrated Circuits, May 24-27, 1998

LARGE SIGNAL MODELLING THROUGH EM AND HB SIMULATIONS

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In this communication, we address the large signal modelling issue by means of Harmonic balance (HB) and Electromagnetic (EM) simulations with application to the design of a tripler with an output frequency @ 250 GHz*. For that purpose, we proceeded by means of the following method. First of all, the active device, which is a Heterostructure Barrier Varactor (HBV) was designed and fabricated having in mind two key requirements, namely a large power handling capability and a strongly non linear capacitance. To this aim, we made use of strained layered heterostructures with a step-like barrier scheme and two epitaxially stacked diodes [1]. On this basis, three types of device configurations have been fabricated and RF tested. Scanning Electron Micrographs of these test samples are shown in Figure 1 (a), (b) and (c) respectively.

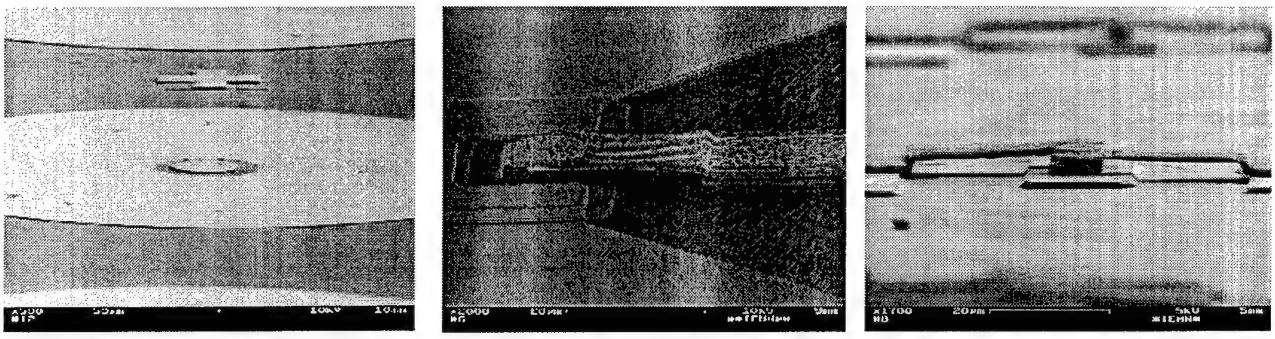
The first test pattern is a coaxial-type consisting of a mesa-etched diode, with a concentric side contact. In this case, the RF probes are positioned directly onto the pads and the intrinsic elements of the diode, namely the capacitance and the series resistance, can be measured without de-embedding techniques and under small signal conditions. Figure 2 illustrates this kind of characterization at the intrinsic level with the variations of the capacitance measured near the pump frequency, @ 85 GHz. The non linearity of the capacitance is very high with a ratio of 5:1 and a voltage handling in excess of 10 V.

The second mask set takes advantage of a coplanar waveguide configuration, with the diodes contacted by means of air bridge and deep etch techniques (see Fig. 1(b)). We considered the structure as a whole including the access and connecting elements. For the de-embedding of these elements, systematic EM and network analysis [2] were carried out by means of the commercial software packages HFSS™ and MDS™ by Hewlett Packard. Figure 3 shows a comparison of the locus of the refection coefficient of an unbiased device plotted on Smith Chart. Excellent agreement is thus obtained between measured and calculated data. At this stage, the diode in its environment [3] can be simulated on one hand by means of lumped intrinsic components, reflecting the capacitance modulation and the resistance to the flow of carriers and on the other hand by a scattering matrix modelling the diode embedding.

At last, we processed a wafer with the layout illustrated in Fig 1(c). Two air-bridged diodes are facing each other, planar integrated with various capping contact geometry. To analyze the large signal properties of the diodes HB simulations of the corresponding circuit were performed. The output data are the expected performance in terms of efficiency and output power and also the optimum matching impedances under large signal conditions. Table 1 summarizes the calculated data, for a 50 μm^2 area diode, assuming two reference planes (i) either at the diode location or (ii) at the connecting pads. As expected, the efficiency and output power are similar in both cases. They are calculated for an input pump power of about 100 mW in such a way that the modulation is full over the available voltage range. In contrast, the optimum source and load impedances are quite different. It remains to know whether such closure impedance can synthesized in a multiplier block. This final stage was performed using EM simulations of the whole multiplier block, at the input and output frequencies. The source impedance results, @ 83GHz, are shown in a Smith Chart plot in Figure 4, in terms of reflection loss versus the matching short circuit position (for a fixed length of the first backshort, the second backshort length is swept a half-wavelength).

[1] E. Lheurette et al. , 'High performance InP-based heterostructure barrier varactor in single and stack configuration', Electronics letters, Vol.32, p. 1417, 1996.
[2] J. Tuovinen and N. R. Erikson, 'Analysis of a1170 GHz frequency doubler with an array of planar diodes' on IEEE Microwave Theory and Techniques , Vol. 43, p. 962, 1995.

* work partially supported by ESA contract #9777/92/NL/PB



(a) (b) (c)

Fig. 1: SEM views of coaxial-type (a), coplanar waveguide type (b) and series type (c) test patterns.

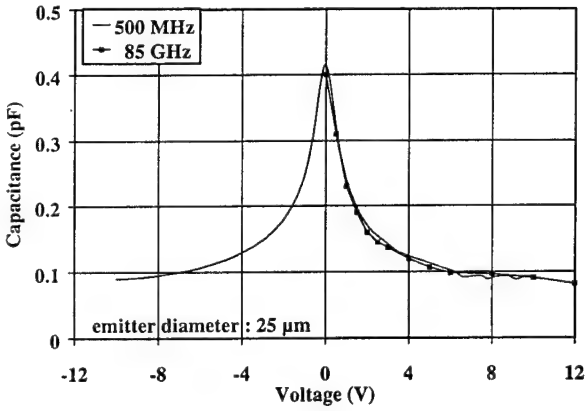


Fig2: C-V curve measured @ 0.5 and 85 GHz

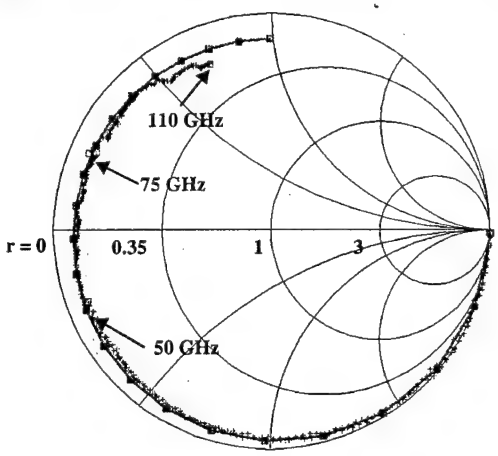
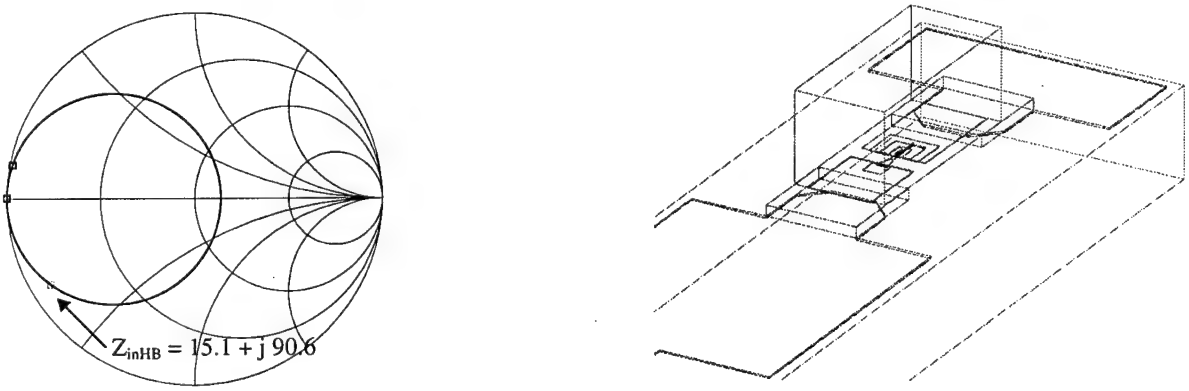


Fig.3 S_{11} versus frequency at zero bias measured (+) and calculated ( ).

DHBV S = 50 µm^2 R_s = 10 Ω	P_{in} (mW)	η(%)	P_{out} (mW)	Z_{load} (Ω)	Z_{source} (Ω)
only intrinsic elements	87.8	22.2	19.5	19 + j 38	15.1 - j 90.6
with extrinsic elements L_f = 75 pH, C_p = 17 fF	85.6	21.9	18.7	19 + j 72	7 - j 36.9

Table 1: Large signal performances in terms of impedance, efficiency and power



(a) (b)

Fig. 4: Smith Chart plot of the diode impedance seen @83 GHz as a function of the matching short circuits position, (a), and layout of the structure simulated with HFSS (b).

A nonlinear, scaleable FET model including temperature dependence and noise effects

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ABSTRACT

This paper describes a new nonlinear spline or functions based FET model, which uses very accurate, measurement based scaling functions. These functions can be used for simulating even temperature and noise behaviour of a device. The model is scaleable with the number and the width of a gate fingers.

THE TOPAS MODEL

In the last few years many papers have been published concentrating either on noise or on temperature simulation [1] or on scaling routines for special effects like dispersion of the trans- and output conductance of a FET [2]. Our TOPAS (TransistOr PArameter Scaleable) called model is based on an accurate 2D spline table based model [3,4], which combines all the above counted effects within one model. The model has been expanded using two dimensional mathematical functions for describing the intrinsic nonlinear elements. The implementation of the TOPAS model into HP-EEofs series IV is consistent. For small input power the large signal simulation turns into the small signal one. This is due to the fact, that small signal capacitances have been replaced by current sources for a large signal simulation

$$i = \frac{\partial Q_2(v_1, v_2)}{\partial t} = C'(v_1, v_2) \cdot \frac{\partial v_1}{\partial t} \qquad (1)$$

Instead of using nonlinear charge sources [5] as

$$Q_2(v_1, v_2) = \int_{v_{10}}^{v_1} C_2(\tilde{v}_1, v_2)\, d\tilde{v}_1 + Q_1(v_2). \qquad (2)$$

SCALING FUNCTIONS

One main requirement for scaling the FETs intrinsic elements is the fact, that the grids of the intrinsic elements do not change their shapes when changing the device. Just the absolute values may change so that one element grid can be calculated from another by multiplying the first grid with a constant number c:

$$c = \frac{\sum_{V_{gs},V_{ds}} \frac{G_x(V_{gs}, V_{ds})}{G_{ref}(V_{gs}, V_{ds})}}{n_{Vgs,Vds}}, \qquad (3)$$

whereby G_{ref} is a reference grid (the reference scaling factor is 1), G_x the scaled element grid and n the number of bias points taken into account. If the grids G_{ref} and G_x have been extracted for different bias points, they must be spline-interpolated to get the same reference of bias points. The second grid (fig. 4) can be calculated from the first grid (fig. 3) by a multiplication with c = 2.89. This value differs just a little from the usually calculated one

$$c_{old} = \frac{8x75\mu m}{4x50\mu m} = 3 \qquad (4)$$

but is more accurate concerning the real device. An example of scaling values of a HEMT device for intrinsic elements is shown in fig. 1. Due to the constant grid shape the intrinsic scaling function $S_I(N,W)$ can be calculated by superimposing both single scaling functions:

$$S_I(N,W) = S_I(N) \cdot S_I(W), \qquad (5)$$

whereby $S_I(X), X = N, W$ can be written as $S_I(X) = a_{IX} X + b_{IX}$. (6)

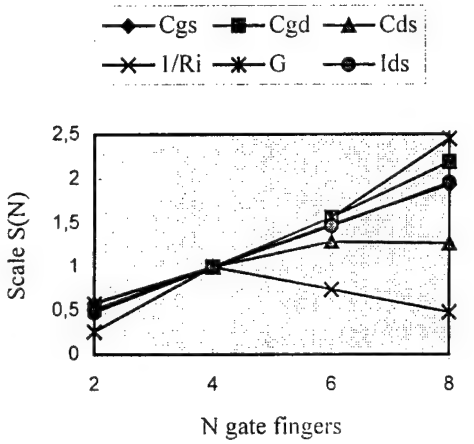

Fig. 1 Scaling of intrinsic elements with number f gate fingers N.

TEMPERATURE DEPENDENCE

For temperature calculations the same proposed scaling functions can be used. Now not different device sizes are scaled but $I_{ds}(V_{gs}, V_{ds})$ of the same device at different temperatures as shown in fig. 2.

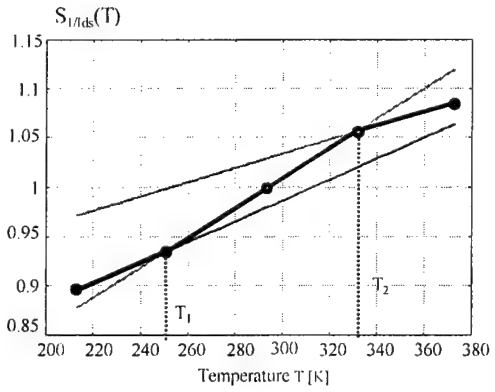

Fig. 2: Scaling coefficients and straight lines.

The temperature behavior including saturation effects (fig. 2) is modeled using eq. 7. Temperature dependence of the intrinsic R_i is been taken care of using eq. 8. As some measurements have shown, the temperature dependence of the capacitances can be neglected.

$$S_{1/I_{DS}}(T) = \begin{cases} a_{1T} \cdot T + b_{1T} & for\ T < T_2 \\ a_{2T} \cdot T + b_{2T} & for\ T_1 \le T < T_2 \\ a_{3T} \cdot T + b_{3T} & for\ T \ge T_2 \end{cases} \quad (7)$$

$$R_i(T) = R_i(T_0) \cdot \left[\gamma_{Ri}(T - T_0) + 1\right] \quad (8)$$

SIMULATION RESULTS

As a simulation example the simulation of the minimum noise figure of a 4×40µm HEMT device is compared to the measurement.

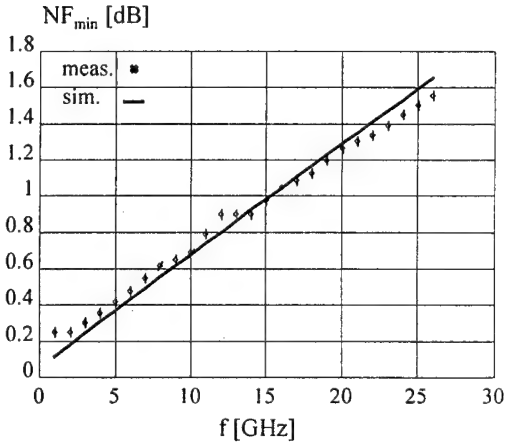

Fig. 3: Simulation vs. measurement of NF_{min} of a 4x40µm HEMT at -0.1 V / 2 V. Model has been scaled from a 4x50µm device.

Although the model has been scaled from a 4×50µm device, measurement and simulation are in perfect agreement.

REFERENCES

[1] F. Sinnesbichler and T. Felgentreff, „Large Signal and Noise Modeling of HEMT devices including Frequency and Temperature Effects," Proc. of the 27th EuMC, Israel, pp.428-431, 1997.

[2] V. I. Cojoracu and T. J. Brazil, „Scaleability of DC/AC non-linear dispersion models for microwave FETs," IEEE-MTT-S International Microwave Symposium Digest, Denver 1997.

[3] R. Follmann, R. Tempel, T. Sporkmann and I. Wolff, „A new spline based FET model for MESFETs and HEMTs," Proc. of the 27th EuMC, Israel, pp. 1360-1366, 1997.

[4] R. Follmann, W. Lütke, R. Tempel and I. Wolff, „A new method for large signal FET modeling for use in MMIC frequency multipliers," IEEE Workshop on "Experimentelly Based FET Device Modelling &

Related Nonlinear Circuit Design", Kassel, pp. 24.1-24.4. 1997.

[5] V. Calvo, A. D. Snider and L. P. Dunleavy, „Resolving capacitor discrepancies between large and small signal FET models," in: *IEEE MTT-S Digest*, pp.1251-1254. 1995.

SiGe HBT in Mixed-Mode Device and Circuit Simulation

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Abstract

We present simulation results for SiGe Heterojunction Bipolar Transistor (HBT), obtained with a hydrodynamic (HD) mixed-mode analysis of a Colpitts oscillator using MINIMOS-NT.

Introduction

Recently the development of heterostructure devices has proceeded with very rapid steps. Analyses of HBTs are of great importance for studying the device characteristics and are prerequisite for further improvements. Accurate simulation of HBT circuits must account for non-local effects and therefore requires hydrodynamic mixed-mode simulation.

Models in MINIMOS-NT

MINIMOS-NT is our two-dimensional device simulator with approved capabilities of simulating devices with complex structure [1]. Splitting the device geometry into segments results in high flexibility which allows, for example, to use a HD model on one segment and a drift diffusion (DD) model on another segment.

For accurate simulation of HBTs for various compound materials the respective temperature and mole fraction dependent models of the physical parameters (e.g. conduction and valence band-edge energies, electron and hole effective masses, effective density of states) on one hand, and of the mobilities on the other hand, were implemented.

The correct modeling of the conduction and valence band-edge energies has basic importance for the simulation results. Band gap narrowing is one of the crucial heavy-doping effects to be considered for bipolar devices. Using the physically-based approach from [2], we implemented a new band gap narrowing model which considers the semiconductor material and the dopant species for arbitrary finite temperatures, and therefore contributes to different changes in the conduction and the valence band-edge energies, respectively. As a particular example we present in Fig. 1 the results for P-doped Si at different temperatures. Note the stronger band gap narrowing at 77K, caused by higher degeneracy. Neglecting of this effect results in an error of about 50%.

As the minority carrier mobility is of considerable importance for modeling advanced n-p-n bipolar transistors, we implemented a new universal low field mobility model [2]. This model distinguishes between majority and minority electron mobilities on one hand, and between different dopant species on the other hand, both as a function of temperature and dopant concentration. This unified treatment is especially useful for accurate device simulation.

The models for the effective density of states take into account a material composition dependent electron and hole effective masses. The effect of valley degeneracy is taken into account for the strained layers.

Results and Conclusion

As a particular example, we simulated a Colpitts oscillator in common emitter configuration. In Fig. 2 we present the output result obtained after transient simulation using a hydrodynamic transport model. Fig. 3 shows the diagram of the oscillator. The SiGe HBT structure used is shown in Fig. 4 where the electron temperature inside the device is presented. The complexity of the HBT structure leaves ample room for

a material dependent performance optimization. Thus, a discussion of constraints is required in order to project performance superiority with respect to certain applications of a particular HBT structure.

Acknowledgment

This work is supported by Siemens AG, Munich, Germany.

References

[1] T. Simlinger, H. Brech, T. Grave, and S. Selberherr. Simulation of Submicron Double-Heterojunction High Electron Mobility Transistors with MINIMOS-NT. *IEEE Trans.Electron Devices*, 44(5):700–707, 1997.

[2] G. Kaiblinger-Grujin, H. Kosina, and S. Selberherr. Influence of the Doping Element on the Electron Mobility in *n*-Silicon. *J.Appl.Phys.*, 15(3), 1998.

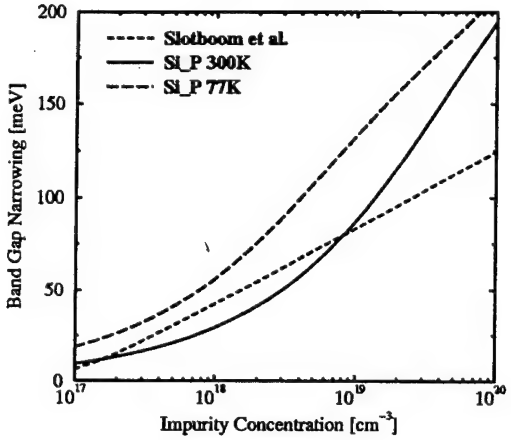

Figure 1: Band gap narrowing versus impurity concentration

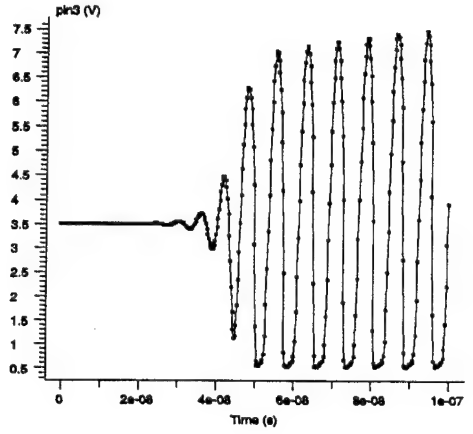

Figure 2: Output voltage versus time

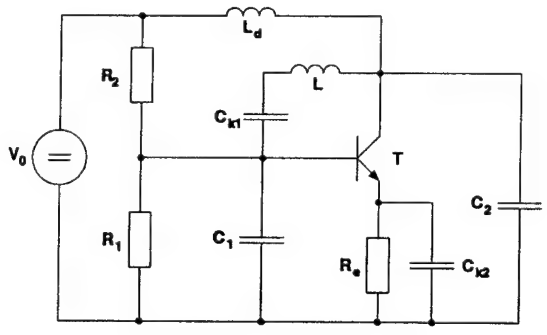

Figure 3: Circuit diagram of a Colpitts oscillator

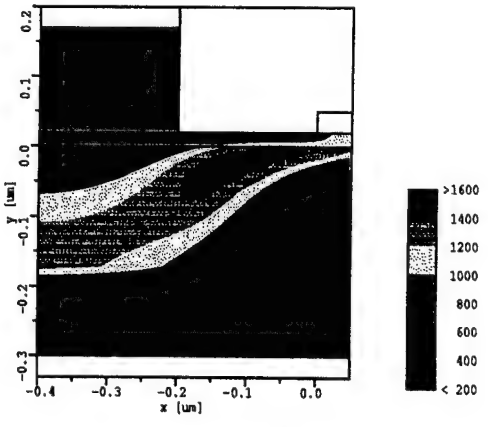

Figure 4: Electron temperature in the device

A new experimental technique for phonon engineering: characterization of InGaAs-based 2DEG channels

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Scattering of confined electrons by confined phonons depends on overlap of their wave-functions, and the scattering rate can be varied on intention by a proper design of electron and phonon quantum wells (phonon engineering, see, e.g. [1] and references therein). This way of controlling electronic properties of two-dimensional electron gas (2DEG) channels is complementary to that provided by modulation doping. Since all scattering mechanisms are taken into account by the electron mobility, an experimental estimate of electron scattering by phonons from the mobility data is hindered by residual and remote impurities, interface roughness and other scattering mechanisms. A separate estimate of the electron scattering by phonons is needed for explicit demonstration of possibilities inherent to phonon engineering.

We propose an experimental technique suitable for controlling electron scattering by phonons independently of elastic scattering mechanisms due to interface roughness, impurities, etc.

The idea of the technique is as follows. Under specified experimental conditions the spectral density of excess noise power emitted by hot electrons $k_B(T_n-T_0)$ is proportional to the power consumed by one electron $e(\mathbf{v}_d\mathbf{E})$. Here k_B is the Boltzmann constant, e is the elementary charge, $\mathbf{v}_d$ is the drift velocity in electric field $\mathbf{E}$, T_0 is the lattice temperature and T_n is the equivalent noise temperature of hot electrons. The coefficient of proportionality

$$\gamma = k_B(T_n-T_0) / e(\mathbf{v}_d\mathbf{E}) \qquad (1)$$

contains the electron energy relaxation time constant τ_ε determined by interaction with phonons.

Frequent electron-electron collisions in 2DEG establish hot-electron distribution governed by the electron temperature T_e available from the energy gain-loss balance: $e(\mathbf{v}_d\mathbf{E}) = (\bar{\varepsilon} - \bar{\varepsilon}_0)/\tau_\varepsilon$ where $\bar{\varepsilon} = k_B T_e$ is the electron mean energy. The transverse noise temperature $T_{n\perp}$ (measured in the direction transverse to the bias current) equals the electron temperature: $T_{n\perp} = T_e$. Consequently,

$$\gamma_\perp = \tau_\varepsilon. \qquad (2)$$

The problem is more complicated if one seeks to determine τ_ε from the noise measured in the direction of current. Now, the longitudinal noise temperature $T_{n\parallel}$ results from the electron temperature T_e and from the contributions appearing due to the bias current: $T_{n\parallel} = T_e(1 + O_\parallel)$. So,

$$\gamma_\parallel = \tau_\varepsilon [1 + O_\parallel(\omega, E)]. \qquad (3)$$

The coefficient $\gamma_\parallel$ approximately equals the energy relaxation time constant τ_ε provided $O_\parallel(\omega, E)$ is small. This can be satisfied in the range of frequencies and electric fields where the hot-electron noise described by the electron temperature dominates over the noise sources which need bias current to manifest themselves (1/f fluctuations, generation-recombination noise, real-space transfer noise, intervalley noise and others). For example, the expression for $O_\parallel(\omega, E)$ has been written down as a function of small-signal mobilities $\mu_\parallel$ and $\mu_\perp$ for a 3DEG model [2]:

$$O_\parallel = 1/4\, T_e/(T_e - T_0)\,(\mu_\parallel/\mu_\perp + \mu_\perp/\mu_\parallel - 2)]. \qquad (4)$$

After Eq.(4) the dimensionless term $O_\parallel < 0.07$ provided $T_e < 4(T_e - T_0)$ and $\mu_\perp/\mu_\parallel < 1.3$.

The longitudinal noise temperature $T_{n\parallel}$ was measured at microwave frequencies for planar-doped InAlAs/InGaAs/InAlAs/InP quantum well channels [3]. The electrons were supplied to the QW in InGaAs by the donor plane located in the InAlAs barrier and separated from the 2DEG by a 3 nm InAlAs spacer. Structure 13Q had a lattice-matched InGaAs channel, structure 14Q contained a pseudomorphic 12 nm InGaAs layer (70 % of InAs) inserted between the spacer and the lattice-matched 30 nm layer of InGaAs. Structure 15Q had no lattice-matched InGaAs layer, the two 2DEG channels were formed in the pseudomorphic 12 nm InGaAs layer (70 % of InAs) by two planes of donors located in the InAlAs barrier layers on both sides of the InGaAs layer.

In the field range below that for real-space-transfer noise in 13Q and 14Q channels (~2 kV/cm for channel 13Q and ~3 kV/cm for channel 14Q) the main source of microwave noise was ascribed to interaction of the confined electrons with the phonons confined inside the InGaAs layer and the interface phonons [3]. The hot-electron real-space-transfer noise was not important in channel 15Q in the range of fields below 3.5 kV/cm, but a superposition of the phonon-related noise and the two-2DEG-channel partition noise was observed at low and intermediate electric fields [3].

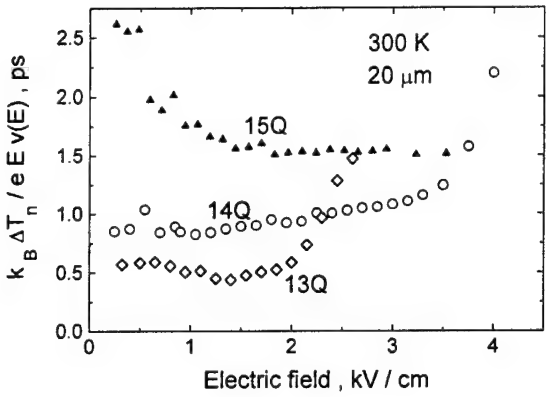

Fig. 1. Experimental data on $\gamma_\parallel$ (see Eqs. (1) and (3)) for different InGaAs-based channels (Table 1). The observed steep increase of $\gamma_\parallel$ at high fields is caused by the onset of the hot-electron real-space-transfer noise (channels 13Q and 14Q). The two-channel partition noise manifests itself in channel 15Q at fields below 1 kV/cm.

Figure 1 presents the field dependence of excess longitudinal noise temperature normalized to the power gained by an electron from the field. A weak (if any) dependence is observed at fields below 2 kV/cm and 3 kV/cm for channels 13Q and 14Q, respectively, and for channel 15Q in the range 1.5 kV/cm < E < 3.5 kV/cm. The deviations from the Ohm law being small in these ranges of field, the energy relaxation time constant τ_ε is estimated neglecting $O_\parallel$ in Eq. (3) with the results listed in Table 1 demonstrating a dependence of τ_ε on phonon quantum well design.

Table 1. Electron mobility and energy relaxation time constant in InGaAs channels at 300 K

Channel	InGaAs layer	μ (cm^2/Vs)	τ_ε (ps)
13Q	lattice-matched	10560	0.5
14Q	pseudomorphic/lattice-matched	11170	0.9
15Q	pseudomorphic	7260	1.5

Acknowledgments

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References

[1] J.Požela, V.Jucienė, A.Namajūnas and K.Požela. *phys.stat.sol.*(b) **204**, 238 (1997).

[2] Sh.M.Kogan and A.Ya.Shul'man. *Sov. Phys. -Solid State* **9**, 1771 (1968).

[3] A.Matulionis, V.Aninkevičius, J.Berntgen, D.Gasquet, et al. *phys.stat.sol.*(b) **204**, 453 (1997).

2D Electron Subband Population and Mobility in a GaAs Quantum Well with a Thin AlGaAs Barrier

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The engineering of confined electron-polar optical phonon scattering rate by inserting a thin AlGaAs barrier inside a GaAs quantum well (QW) allows to achieve the photoexcited electron subband population inversion, to create infrared lasers and to tune electron mobility in field-effect transistor channels. The AlGaAs barrier between coupled QW's is a good tool for tuning electrical and optical parameters of heterostructures.

The electron subband energy and population engineering by inserting a thin AlGaAs barrier inside a GaAs QW is considered. The specific voltage across coupled QW's which arises due to the asymmetric deformation of electron wave function is estimated. The simplified analytical model for confined and interface polar optical phonons in the double barrier GaAs QW with the inserted AlGaAs barrier is described. The electron–phonon scattering rates, the electron mobility and the photoexcited electron subband population as functions of the position of AlGaAs barrier in the asymmetric coupled QW's are considered.

The inserted AlGaAs barrier changes the photoexcited hot electron distribution between QW subbands. The inversion of the photoexcited electron subband population occurs when the intersubband energy separation becomes less than the confined or interface polar optical phonon energy. The electron intersubband redistribution leads to the anomalies in photoluminescence spectra which have been observed experimentally.

LOW-FREQUENCY NOISE STUDIES IN AlGaN/GaN HEMT´s

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The low-frequency noise characteristics of $Al_{0.15}Ga_{0.75}N/GaN$ single heterostructure high electron mobility transistors, for two contact device processings and gate widths (W), have been studied. Heterostructures were grown on sapphire substrates by MOVPE, and the active device consists of a 500Å-thick GaN layer, a 30Å-thick AlGaN spacer, and a 300Å-thick n-doped AlGaN barrier layer. The gates in type A (W=50μm) and type B devices (W=100μm) are equidistant from source and drain, while in type C devices (W=50μm), with a different ohmic contact processing, the gate is closer to the drain. As a result type C devices show a very high contact resistivity and a poor gate current-voltage characteristic.

Noise measurements vs V_{GS} were performed under a V_{DS}=50mV. 1/f noise spectrum was obtained at 300K in the voltage range under study (-3V, 1.5V) , that follows the Hooge dependence[1]. Figure 1 shows the drain voltage noise (S_V), at f=10 Hz, where three regions are observed as the gate voltage is increased . For V_{GS} from -3V to 0V (region I), the channel resistance and the channel noise dominate. A power law dependence between mobility (μ) and sheet carrier density (n_S), $\mu \propto n_S^2$, is observed and explained by the screening effect. The noise measurements show a dependence of the Hooge parameter (α_H) with V_{GS}, and hence with n_S, which have been correlated with the dependence of the Coulomb scattering rate on n_S [2]. A value of the Hooge constant of $\alpha_H=5\cdot10^{-4}$ was found at V_{GS}=0V.

The noise measured in regions II (0V,1.25V) and III (V_{GS}>1.25V) is dominated by the contact and the gate, respectively, as shown below. Figure 2 shows the voltage noise in the three devices for two measurement configurations: V_{DS}=50mV (open symbols) and floating drain (solid symbols).

Measurements in region II, under V_{DS}=50mV, provide a constant S_V with V_{GS} for all the devices. Furthermore, the same noise level is obtained for type A and B devices, so that S_V cannot be originated in the channel, barrier or ungated zones as it does not scale with the device area. The noise sources are suggested to be located at the drain and source contacts. The increased S_V observed in type C devices confirms this attribution, due to its higher contact resistivity.

The influence of the gate contact quality on the noise power has also been studied. Noise measurements were performed under floating drain configuration (figure 2), in order to obtain the contribution of the gate current noise to the floating drain. The voltage noise spectrum shows an I_{GS}^{β} relationship, β being proportional to the ideality factor of the I-V gate curve. This behaviour can be understood in terms of a model that associates the noise spectral density in Schottky diodes with fluctuations in the recombination gate current[3]. For type C devices, the influence of the gate fluctuations in the drain-source noise begins at lower gate voltages, due to its leaky gate current-voltage characteristic.

In conclusion, 1/f noise has been observed in AlGaN/GaN HEMT´s. For increasing V_{GS}, the noise is dominated by Coulomb scattering in the channel, the ohmic contacts and the gate leakage current.

[1] F. N. Hooge, Phy. Lett. **29A,** 139 (1969)
[2] M.A. Py, H.J. Buehlmann, J. Appl. Phys. **80** (3), 1583 (1996)
[3] A. van der Ziel, Procc. IEEE **58,** 1178 (1970)

Figures

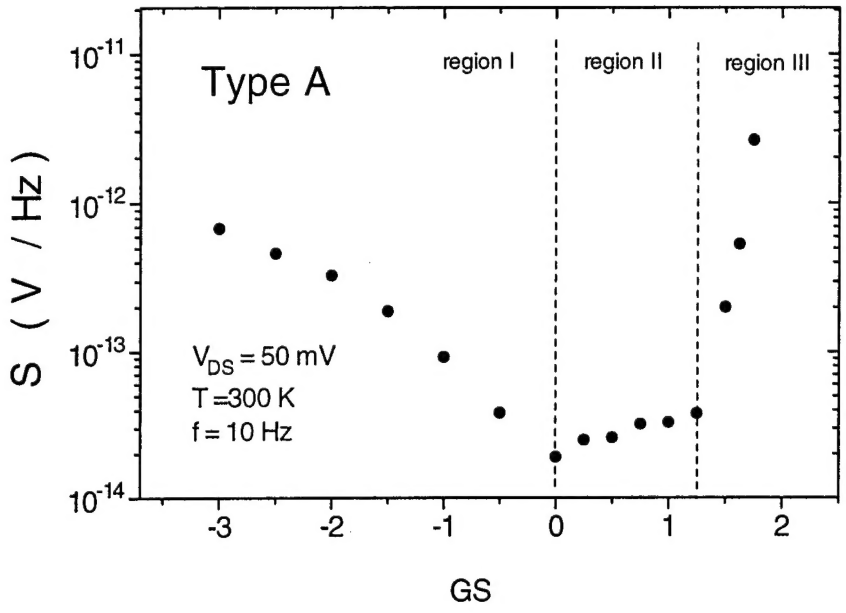

Figure 1. Drain noise power density (S_V) versus gate voltage (V_{GS})

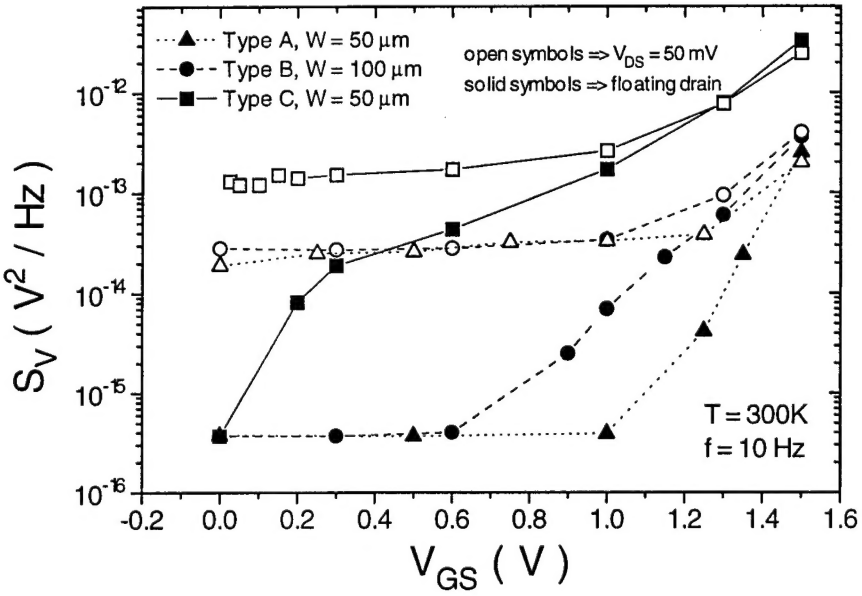

Figure 2. Influence of the gate noise and the drain-source contact noise.

Mobility dependence of the low frequency noise of 2DEG structures

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High speed semiconductor devices based on InP substrates gain more and more in interest for modern telecommunication. Particularly, heterostructure field-effect transistors (HFETs) having $In_xGa_{1-x}As$ quantum well channels exhibit excellent microwave performance due to the spatial separation of the electron-supplying layer and the two dimensional electron gas (2DEG) channel. However, these devices suffer from their low-frequency (LF) noise, which is a hampering limitation of the device performance for applications such as wideband amplifiers or nonlinear circuits having noise upconversion. Till today, the origin of the 1/f noise is not well understood. First investigations concerning the mobility dependence of the Hooge parameter α_H in homogeneously doped bulk samples were performed by Hooge several years ago [1,2]. Evaluating the LF noise measurements of a series of homogeneous n-GaAs and n-InP samples with different doping concentrations confirmed the relation between α_H and μ according to eq. (1).

$$\frac{S_V}{V^2} = \frac{\alpha_{H\,tot}}{N \cdot f} \qquad \text{with} \qquad \alpha_{tot} = \left(\frac{\mu_{tot}}{\mu_{phon}}\right)^2 \cdot \alpha_{phon} \tag{1}$$

S_V/V^2 = normalized spectral 1/f noise, N = number of free charges, μ = mobility, α_H = Hooge parameter, Index 'phon' = phonon scattering, 'tot' = total measured quantity.

In this equation, μ_{phon} and $\alpha_{H\,phon}$ are the mobility and the Hooge parameter, respectively, for undoped samples, where only phonon scattering is present. According to [1, 2], the Hooge parameters of undoped homogeneous GaAs or InP at room temperature is about $2\text{-}3\cdot10^{-3}$. With increasing doping concentration, the resulting Hooge parameter $\alpha_{H\,tot}$ decreases with the square of the mobility ratio $(\mu_{tot}/\mu_{phon})^2$ due to decreasing mobility. In contrast to these homogeneously doped samples, no systematic investigation on the mobility dependence of the Hooge parameter in 2DEG has been published so far. In order to elucidate this problem, the LF noise properties of eight different Al-free and Al-containing HEMT structures based on semi-insulating InP substrate with InGaAs 2DEG channels has been investigated. The relevant properties like In content in the channel, channel thickness, sheet carrier concentration n_S, upper and lower conduction band offset, mobility μ and measured Hooge parameter α_H are listed in table 1. The three Al-free InP/InGaAs/InP samples H38, H40 and H42 have the same layer design with comparable sheet carrier concentrations and differ only in the In content in the channel. This series of samples shows a measured Hooge parameter, which decreases with increasing conduction band offset and increasing mobility. A similar behavior is observed for the Al-containing InAlAs/InGaAs heterostructures. The samples DU335 and DU387 or 13Q and 14Q have comparable sheet concentrations in pairs. A comparison yields the same conclusion. In particular, the implementation of the Al-rich thin spacer in sample DU335 with its increased conduction band offset results in a halving of α_H. Sample 15Q with a thin strained channel and a high sheet carrier concentration of $n_S = 4.12\cdot10^{12}\ cm^{-2}$ also shows this strong correlation between μ and α_H. This high sheet concentration in the thin channel results in a low mobility and thus in a higher Hooge parameter. In Fig. 1, the Hooge parameters α_H of the investigated samples versus channel mobilities are shown. In spite of the different layer designs, conduction band offsets and sheet carrier concentrations, this double logarithmic diagram gives a clear dependence between α_H and μ. Here, the relation $\alpha_H \sim \mu^{-2.6}$ was observed. The lowest Hooge parameter $\alpha_H = 1.5\cdot10^{-5}$ was found in the samples 14Q and DU335, both having the highest mobilities. In contrast to this, the Al-free samples H38, H40 and H42, which have a poorer confinement due to rather low conduction band offsets, achieved the highest Hooge parameters. But nevertheless, the correlation between μ and α_H of all samples with InGaAs 2DEG channels and arbitrary designs seems to be described exactly with

$$\alpha_H = 8.05\cdot10^5 \cdot \left(\frac{\mu_{tot}}{1\,\frac{cm^2}{Vs}}\right)^{-2.6} \tag{2}$$

		In content in the channel	channel thickness d [nm]	sheet concentration n_S [10^{12} cm^{-2}]	conduction band offset at the upper/lower channel ΔE_C [eV]	mobility μ [cm^2/Vs]	Hooge parameter α_H [10^{-5}]
Al-free	H38	53%	12	1.53	0.26	6470	9
	H40	60%	12	1.68	0.29	7060	7
	H42	67%	12	1.67	0.32	7840	5
Al-containing	DU387	53%	24	3.3	0.45	10400	3
	DU335	53%	20	2.7	0.84 (spacer 70% Al) / 0.45	11500	1.5
	13Q	53%	30	2.38	0.45	10560	3.2
	14Q	70% / 53%	12 / 30	2.28	0.55 / 0.45	11170	1.5
	15Q	70%	12	4.12	0.55	7260	4.5

Tab. 1: Relevant properties of investigated Al-free and Al-containing InP-based 2DEG structures at 300 K.

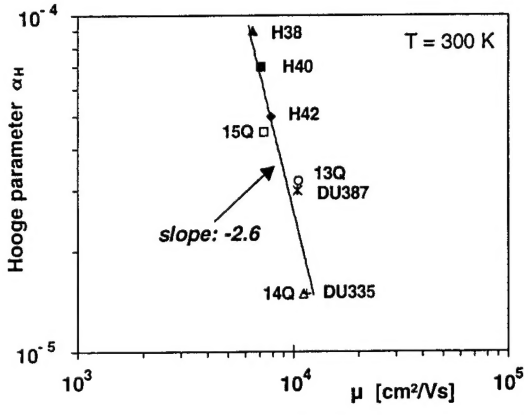

Fig. 1: Hooge parameters of different InP-based 2DEG structures having InGaAs channels in dependence on the mobility obtained from room temperature LF noise measurements.

These investigations presented for the first time show that the 1/f noise in various 2DEG with InGaAs channels, where only phonon scattering is present, depends in a completely different way on the measured mobility μ_{tot} than homogeneously doped samples. In the following, the strong mobility dependence of the Hooge parameter in 2DEG will be discussed considering various design parameters. This effect can be explained by the different conduction band discontinuities and penetration depths of free carriers into the barriers. It is generally known, that the smaller is the conduction band offset of the heterostructure, the higher is the penetration depth of charges into the barriers. This leads to a parallel conduction between the charges in the high mobility 2DEG channel with its low Hooge parameter and those in the barriers. According to [1, 2], the Hooge parameter for the barriers ($\alpha_{H\,phon}$ of bulk material) is about two orders of magnitude higher than the measured Hooge parameters obtained from 2DEG structures. The total measured normalized spectral LF noise due to parallel conduction can be calculated as follows:

$$\frac{S_V}{V^2}=\frac{\alpha_{H\,tot}}{N_{tot}\,f}=\left(\frac{R_{chan}}{R_{barr}+R_{chan}}\right)^2\cdot\frac{\alpha_{H\,barr}}{N_{barr}\,f}+\left(\frac{R_{barr}}{R_{barr}+R_{chan}}\right)^2\cdot\frac{\alpha_{H\,chan}}{N_{chan}\,f} \qquad (3)$$

(index 'chan' for the channel and index 'barr' for the barrier properties)

Even if only a fraction of the total number of charges penetrates into the channel barriers they can still contribute to the noise because of the high $\alpha_{H\,barr}$. This explains, why Al-free structures with shallow InP/InGaAs quantum wells show a worse LF noise behavior than deeper InAlAs/InGaAs ones. Additionally the In content in the channel affects the Hooge parameter. Using a slightly increased In content in the InGaAs channel, the potential step can be increased and the electron density distribution function penetrates shallower into the barriers, hence increasing the mobility and decreasing α_H. On the other hand, designing such strained channels limits the channel thickness. In thin channels, the electrons are not only present in the first energy level, but also in the higher energy levels. This leads to an interaction between these levels and results in a reduced mobility and high Hooge parameter. Therefore, splitted channels are much more suitable for LF noise applications. This kind of channel design allows a combination of a wide channel with a high upper potential step, where only the first energy level is populated. Another possibility to minimize α_H is to introduce a thin strained spacer (sample DU335) with a higher conduction band offset compared to unstrained $In_{0.52}Al_{0.48}As$.

The performed experiments showed a strong correlation between μ and α_H for 2DEG structures, depending on the channel design. The specifications for 2DEG structures with optimized Hooge parameter are a minimum penetration depth and an occupation of the first energy level only. Finally the question arises how the results found for 2DEG structures correlate with Hooge's theory for homogeneously doped samples. If only phonon scattering is present in undoped homogeneous GaAs or InP, the Hooge parameter $\alpha_{H\,phon}$, which is identical with the measured one $\alpha_{H\,tot}$, is about $2\text{-}3\cdot10^{-3}$ at room temperature. On the contrary, Hooge parameters have been obtained from 2DEG structures, which were up to two orders of magnitude lower (depending on structure design). This discrepancy between the high $\alpha_{H\,phon}$ values in homogeneous undoped semiconductors and the low measured ones in 2DEG, where only phonon scattering is present, is not clear so far [3]. In our opinion, there is a difference between mobility fluctuations (and therefore α_H) in homogeneous material and in 2DEG due to the different degrees of freedom. The electrons in 2DEG are limited to scatter in only two dimensions, which should result in a lower α_H than the Hooge parameter of three-dimensional scattering processes in bulk material. Regarding the achieved maximum mobilities of the investigated structures, a further decrease of the observed Hooge parameter α_H to values below $1.5\cdot10^{-5}$ at room temperature is hardly possible. This value seems to be the Hooge parameter due to lattice scattering in perfect 2DEG.

References

[1] F.N. Hooge, IEEE Transactions on Electron Devices, vol. 41, p. 1926, 1994.
[2] X.Y. Chen and M.R. Leys, , Solid-State Electronics, vol. 39, p. 1149, 1996.
[3] private communication from F.N. Hooge, 1997.